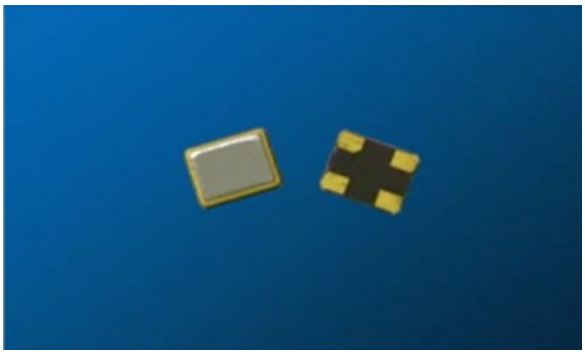
GXL GSP1 series

1.8, 2.5, 3.3 volt CMOS Oscillator



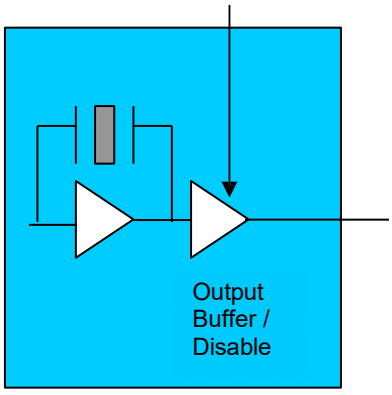
GSP1 Crystal Oscillator

Features

- Quick delivery
- CMOS output
- 3.2mm x 2.5mm x 1.2 mm
- Output frequencies to 200.00 MHz
- Tri-state output for board test and debug
- -55/125 or –40/85°C operating temperature
- Gold over nickel contact pads
- Hermetically sealed ceramic SMD package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

- SONET/SDH/DWDM
- Ethernet, Gigabit Ethernet
- Storage Area Network
- Digital Video
- Broadband Access
- Microprocessors/DSP/FPGA



f_o

Description

GXL's GSP1 Crystal Oscillator (XO) is quartz stabilized square wave generator with a CMOS output, operating from a 1.8, 2.5 or 3.3 volt supply.
The GSP1 utilized a high performance, low frequency quartz resonator followed by a custom ASIC to synthesize the output frequency.

Table 1. Electrical Performance, 3.3V option					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	0.8		200.000	MHz
Operating Supply Voltage [1]	V_{DD}	2.97	3.3	3.63	V
Absolute Maximum Operating Voltage		-0.5		5.0	V
Supply Current, Output Enabled	I_{DD}				mA
<30 MHz				10	
30.01 to 75 MHz				15	
75.01 to 133 MHz				20	
133.01 to 200 MHz				25	
Supply Current, Output disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High [2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low [2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	8			mA
Output Logic Low Drive	I_{OL}	8			mA
Output Rise/Fall Time [2]	t_R/t_F			5	ns
Duty Cycle [3] *(ordering option)*	SYM	45/55			%
Operating Temperature (*ordering option*)		-55/125 or –40/85			°C
Storage Temperature		-55		125	°C
Stability [4] (*ordering option)*		±50, ±100			ppm
Output Enable/Disable [5]					V
Output Enabled		2.0			
Output Disabled				0.5	
Internal Enable Pull-Up resistor [5]			100		Kohm
Start-up time				10	ms

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the operating conditions under which these parameters are tested and specified. For Fo>90MHz, rise and fall time is measured 20 to 80%.
3. Symmetry is measured defined as On Time/Period.
4. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
5. Output will be enabled if enable/disable is left open.

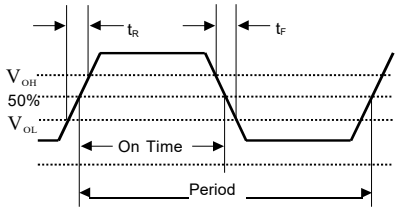


Figure 1. Output Waveform

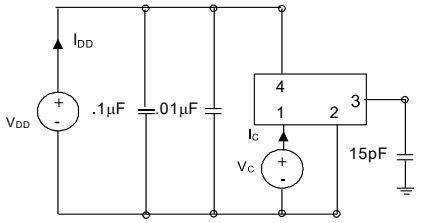


Figure 2. Typical Output Test Conditions (25±5°C)

Table 2. Electrical Performance, 2.5V option					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	0.8		166.000	MHz
Operating Supply Voltage [1]	V_{DD}	2.25	2.5	2.75	V
Absolute Maximum Voltage		-0.5		5.0	V
Supply Current, Output Enabled	I_{DD}				mA
< 30 MHz				8.0	
30.01 to 75 MHz				10.0	
75.01 to 166 MHz				15.0	
Supply Current, Out disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High [2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low [2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	4			mA
Output Logic Low Drive	I_{OL}	4			mA
Output Logic High Drive [3]	I_{OH}	8			mA
Output Logic Low Drive [3]	I_{OL}	8			mA
Output Rise/Fall Time [2]	t_R/t_F			5	ns
Duty Cycle [4] *(ordering option)*	SYM	45/55			%
Operating Temperature (*ordering option*)		-55/125 or –40/85			°C
Storage Temperature		-55		125	°C
Stability [5] (*ordering option)*		±50, ±100			ppm
Output Enable/Disable [6]					V
Output Enabled		1.75			
Output Disabled				0.5	
Internal Enable Pull-Up resistor [6]			100		Kohm
Start-up time				10	ms

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 3 defines these parameters. Figure 4 illustrates the operating conditions under which these parameters are tested and specified.
3. Overtone designs, output frequencies>35MHz.
4. Symmetry is measured defined as On Time/Period.
5. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
6. Output will be enabled if enable/disable is left open.

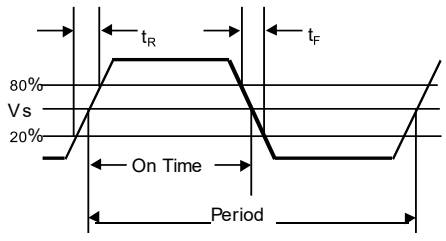


Figure 3. Output Waveform

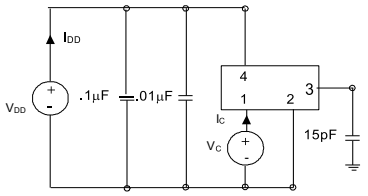


Figure 4. Typical Output Test Conditions (25±5°C)

Table 3. Electrical Performance, 1.8V option					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	0.8		133.00	MHz
Operating Supply Voltage [1]	V_{DD}	1.62	1.8	1.98	V
Absolute Maximum Voltage		-0.5		3.6	V
Supply Current, Output Enabled	I_{DD}				mA
< 30 MHz				6	
30.01 to 75 MHz				8	
75.01 to 133 MHz				12	
Supply Current, Out disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High [2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low [2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	2.8			mA
Output Logic Low Drive	I_{OL}	2.8			mA
Output Logic High Drive [3]	I_{OH}	8			mA
Output Logic Low Drive [3]	I_{OL}	8			mA
Output Rise/Fall Time [2]	t_R/t_F			5	ns
Duty Cycle [4] (*ordering option*)	SYM	45/55			%
Operating temperature (*ordering option*)		-55/125 or –40/85			°C
Storage Temperature		-55		125	°C
Stability [5] (*ordering option*)		±50, ±100			ppm
Output Enable/Disable [6]					V
Output Enabled		1.26			
Output Disabled				0.5	
Internal Enable Pull-Up resistor [6]			1		Mohm
Start-up time				10	ms

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 5 defines these parameters. Figure 6 illustrates the operating conditions under which parameters are tested/specified.
3. Overtone designs, output frequencies>35MHz.
4. Symmetry is measured defined as On Time/Period.
5. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
6. Output will be enabled if enable/disable is left open.

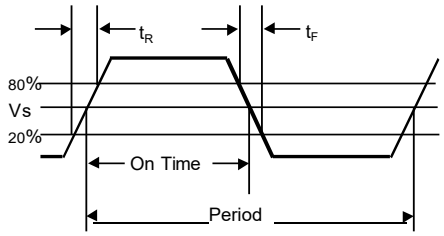


Figure 5. Output Waveform

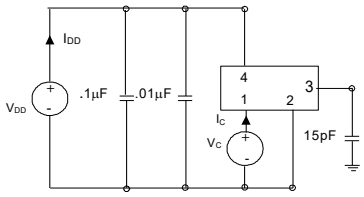


Figure 6. Typical Output Test Conditions (25±5°C)

Enable/Disable Functional Description

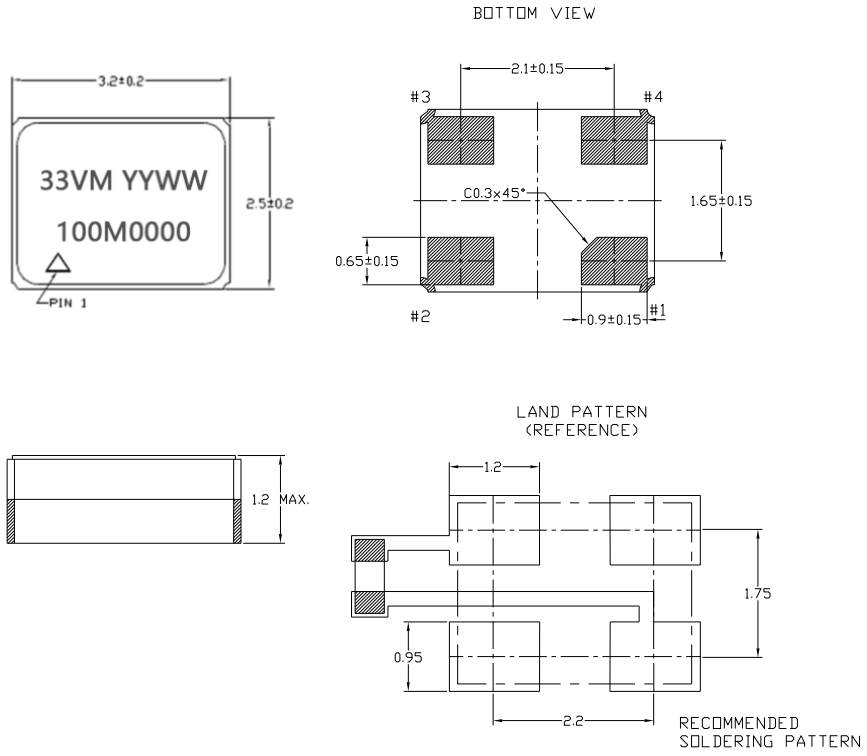
Under normal operation the Enable/Disable is left open or set to a logic high state. When the E/D is set to a logic low, the oscillator stops and the output is in a high impedance state. This helps reduce power consumption as well as facilitating board testing and troubleshooting.

Tri-state Functional Description

Under normal operation the tri-state is left open or set to a logic high state. When the tri-state is set to a logic low, the oscillator remains active but the output buffer is in a high impedance state. This helps facilitate board testing and troubleshooting.

Table 4. Outline Diagrams, Pad Layout and Pin Out

Pin #	Symbol	Function
1	E/D or NC	Tri-state, Enable/Disable or NC
2	GND	Electrical and Case Ground
3	f_O	Output Frequency
4	V_{DD}	Supply Voltage



Contact Pads are gold over nickel

Figure 9, Package drawing

Ordering Information

GSP1 - 33V - M - 100M0000

Product Family
Crystal Oscillator

Output Frequency

Voltage Options

33V: +3.3 Vdc +/-10%, 15pF

25V: +2.5 Vdc +/-10%, 15pF

18V: +1. 8Vdc +/-10%, 15pF

Stability Options

F: ±50ppm, -40 to 85°C

H: ±50ppm, -55 to 85°C

M: ±100ppm, -55 to 125°C