Features

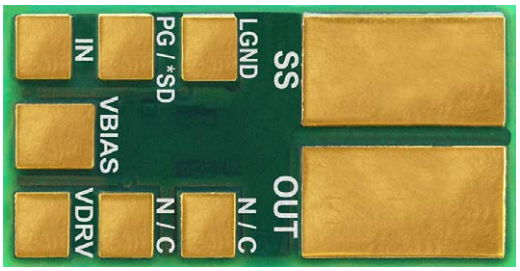
- **50 V_{DC}/12 A De-Rated Operation (100 V_{DC} Capable)**
- **Single Independent Low-Side Power Driver**
- **100 V_{DC} eGaN® HEMT Output Power Switch**
- **100 V_{DC} Power Schottky Catch Diode**
- **Gate Bias UVLO Detection, Protection and Reporting**
- Bidirectional Shutdown Input/Power Good Output
- Internal V_{BIAS} Overvoltage Protection
- **High Speed Capability: 3.0 MHz+**
- Rugged Compact Molded SMT Package "Pillar" I/O Pads
- eGaN® Switching Elements
- No Bipolar Technology
- Compact 0.500 x 0.375 x 0.135" Size

Radiation Hardness

- Guaranteed Total Ionizing Dose:
  - Rated to 100kRad
- Single Event:
- SEE immunity for LET(Si) of ~83.7 MeV/mg/cm^2 With V_{DS} up to 100% of *Rated Breakdown
- Neutron Fluence:
  - Maintains Specification Up to 1 x 10^{13} N/cm^2

Application

- Synchronous Rectification
- Power Switches/Actuators
- Multi-Phase Motor Drivers
- Commercial Satellite EPS & Avionics
- High Speed DC-DC Conversion



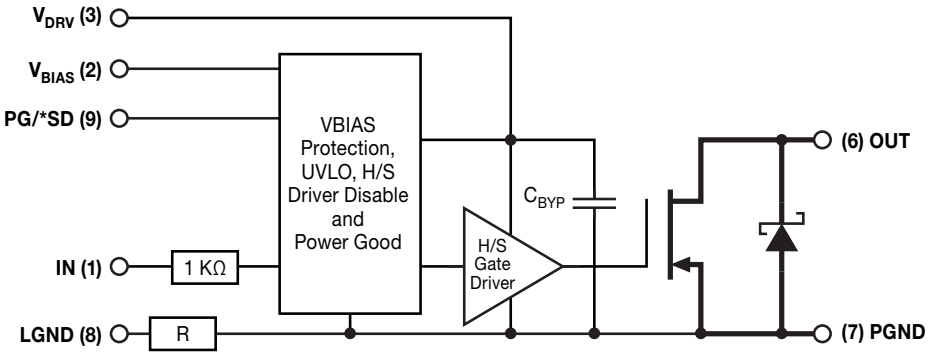
FBS-GAM01-P-R50

Radiation-Hardened 50 V_{DC}/12 A Single Low-Side Power Driver Module

Description

EPC Space's "GaN Driving GaN Technology" **Radiation-Hardened FBS-GAM01-P-R50 Single Low Side Power Driver Module** incorporates eGaN® switching power HEMTs. These devices are integrated with EPC Space's FDA10N30X output power eGaN® HEMT switch, output clamp Schottky diode, and optimally driven by **high-speed Gate Drive Circuit consisting entirely of eGaN® switching elements**. Further +5V Input V_{BIAS} over-voltage clamping protection with V_{BIAS} under- voltage driver disable and reporting are contained within an innovative, space-efficient, 9 pin SMT Over-Molded Epoxy Package. Data sheet post radiation guaranteed with **100% Wafer by Wafer eGaN® element** Radiation Hardness-Assured (RHA) validation. Circuit design under US Patent #10,122,274 B2 (Commerce Export Rated 9A515.e.1)

FBS-GAM01-P-R50 Functional Block Diagram

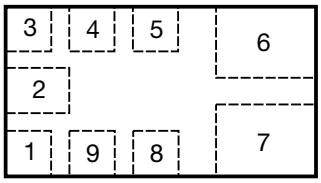


(Pins 4 and 5 are No Connect)

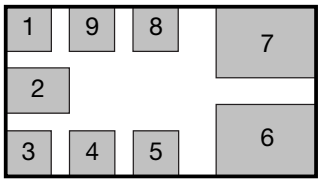
FBS-GAM01-P-R50 Functional Block Diagram

9 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



FBS-GAM01-P-R50 Configuration and Pin Assignment Table

Pin #	Pin Name	Input/Output	Pin Function
1	IN	|	Power Switch Gate Driver Logic Input
2	V_{BIAS}	--	+5 V_{DC} Gate Driver Power Supply Bias Input Voltage
3	V_{DRV}	--	Protected Gate Driver Internal Power Supply Bias Voltage
4	N/C	--	No Internal Connection
5	N/C	--	No Internal Connection
6	OUT	O	Power Switch Open Drain Output (High Current)
7	SS	--	Power Supply Ground/Return, 0 V_{DC} (High Current)
8	LGND	--	Logic Ground/Return, 0 V_{DC}
9	PG/*SD	I/O	Power Good Output/Shutdown Input

Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions		Value	Units
V_{DS}	Power Switch Drain to Source Voltage (Note 1)	Fully De-Rated	50	V
		Component Capable	100	
I_D	Continuous Drain Current		12	A
V_{BIAS}	Gate Driver Bias Supply Voltage	DC	-0.3 to 6.0	V
		50 ms	7.5	
IN	Logic Input Voltage		-0.3 to 5.5	
T_{STG}	Storage Junction Temperature Range		-55 to +140	°C
T_J	Operating Junction Temperature Range		-55 to +130	
T_C	Case Operating Temperature Range		-55 to +110	
T_{sol}	Package Mounting Surface Temperature		230	
ESD	ESD Class Level (HBM)		1	A

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JC}$	Thermal Resistance Junction to Case, eGaN® Power Switch (Note 3)	8.5	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case, Clamp Schottky Diode (Note 3)	30	

OUT Power Switch Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
OUT Driver Output Leakage Current	I_{IL}	V_{DS} = 25 V_{DC}; IN = 0.8 V_{DC} (Note 1)	T_C = 25°C		10	125	µA
			T_C = 110°C		75	250	
		V_{DS} = 50 V_{DC}; IN = 0.8 V_{DC} (Note 1)	T_C = 25°C		15	170	
			T_C = 110°C		100	505	
		V_{DS} = 100 V_{DC}; IN = 0.8 V_{DC} (Note 1)	T_C = 25°C		75		µA
			T_C = 110°C		550		
OUT Driver ON-State Resistance	$R_{DS(on)}$	IN = 3 V_{DC}; I_D = 12 A (Note 1, 2)	T_C = 25°C		8	10	mΩ
			T_C = 110°C		10	15	
			T_C = -55°C		5.5	9	
OUT Driver Source-Drain Clamping Voltage	V_{SD}	IN = 0.8 V_{DC}; I_D = 12 A (Note 1, 2)	T_C = 25°C		0.75	0.90	V
			T_C = 110°C		0.60	0.75	
			T_C = -55°C		0.95	1.15	

IN Logic Input Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
Low Logic Level Input Voltage	V_{IL}	V_{BIAS} = 5 V_{DC} (Note 4)				0.8	V
High Logic Level Input Voltage	V_{IH}	V_{BIAS} = 5 V_{DC} (Note 5)		2.9			V
Low Logic Level Input Current	I_{IL}	V_{BIAS} = 5 V_{DC}, V_{IL} = 0.4 V_{DC}	T_C = 25°C	-5	+/-1	5	µA
			T_C = 110°C	-45	+/-10	45	
High Logic Level Input Current	I_{IH}	V_{BIAS} = 5 V_{DC}, V_H = 5 V_{DC}	T_C = 25°C	-5	+/-1	5	
			T_C = 110°C	-45	+/-10	45	

V_{BIAS} Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} Recommended Operating Voltage Range	V_{BIAS}	(Note 3)	4.5		5.5	V
V_{BIAS} Operating Current	I_{BIAS}	V_{BIAS} = 5.5 V_{DC}		6.5	10.5	mA
		V_{BIAS} = 7.5 V_{DC}		90		

PG Functional Static Electrical Characteristics *(-55°C ≤ T_C ≤ 110°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} UVLO Rising Threshold	UVLO+	(Notes 6, 7, 8, 9)			4.45	V
V_{BIAS} UVLO Falling Threshold	UVLO-		2.95			
UVLO Hysteresis	(UVLO+) - (UVLO-)			0.2		

PG Logic Output Static Electrical Characteristics *(-55°C ≤ T_C ≤ 110°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Low Logic Level Output Voltage	V_{OL}	V_{BIAS} = 5 V_{DC} (Notes 6, 7 and 8)			0.2	V
High Logic Level Output Voltage	V_{OH}	V_{BIAS} = 5 V_{DC} (Notes 6, 7 and 8)	3.5			V
Low Logic Level Output Current	I_{OL}	V_{BIAS} = 5 V_{DC} (Note 6)			10	mA
High Logic Level Output Leakage Current	I_{OH}	V_{BIAS} = 5 V_{DC}, PG = 5.5 V_{DC} (Note 6)		100		µA

OUT Power Switch Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
IN-to-OUT Turn-ON Delay Time	$t_{d(on)}$	V_{DS} = 25 V_{DC}; I_D = 12 A (See Switching Figures)		45		ns
OUT Rise Time	t_r			10		
IN-to-OUT Turn-OFF Delay Time	$t_{d(off)}$			45		
OUT Fall Time	t_f			12		

Module Static and Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Output Capacitance (Out-PGND)	C_{OUT}	$V_{(OUT)}$ = 5 V_{DC}, f = 1 MHz		1150		pF
		$V_{(OUT)}$ = 50 V_{DC}, f = 1 MHz		500		
Dynamic Gate/Driver Losses	P_{GD}	V_{BIAS} = 5 V_{DC}		21		mW/ MHz
Schottky Output Diode ON-Time	t_{on}	I_F = 12 A (Note 3), f_s = 1 MHz			100	ns
Minimum Switching Frequency	f_s	V_{DS} = 25 V_{DC}; I_D = 12 A (Note 3)	0			Hz
Maximum Switching Frequency				3.0		MHz
LGND-PGND Resistance	R_S			1		Ω

Specification Notes

1.) V_{BIAS} = +5 V_{DC}, PGND = LGND = 0 V_{DC}.

2.) Measured using 4-Wire (Kelvin) sensing techniques.

3.) Guaranteed by design. Not tested in production.

4.) When the logic input (IN) is at the low input voltage level the power output (OUT) is guaranteed to be OFF (high impedance).

5.) When the logic input (IN) is at the high input voltage level the power output (OUT) is guaranteed to be ON (low impedance).

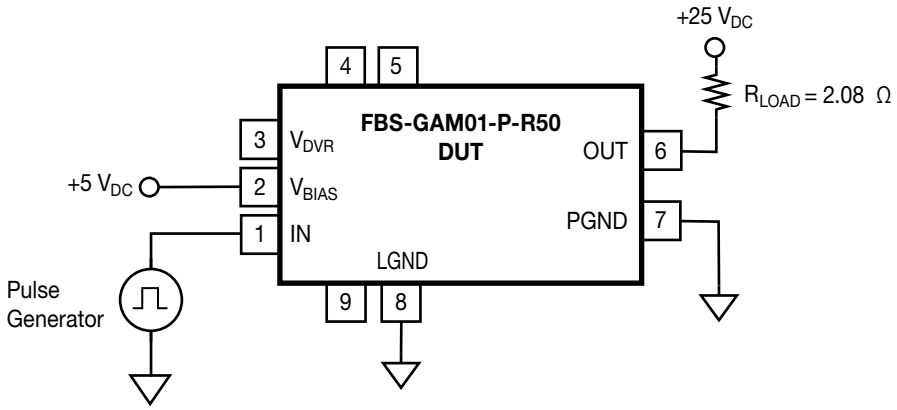
6.) PG/*SD is bidirectional input/output pin: It is a Shutdown input when pulled to LGND using an open-drain/collector; and it is a Power Good output referenced to LGND. For either the SD or PG function, this pin should be pulled up to V_{DRV} with a 4.7 kΩ resistor.

7.) Parameter measured with a 4.7 kΩ pull-up resistor between PG and V_{DRV}.

8.) PG is at a low level when V_{BIAS} is below the UVLO- (falling) threshold level and PG is at a high level when V_{BIAS} is above the UVLO+ (rising) threshold level.

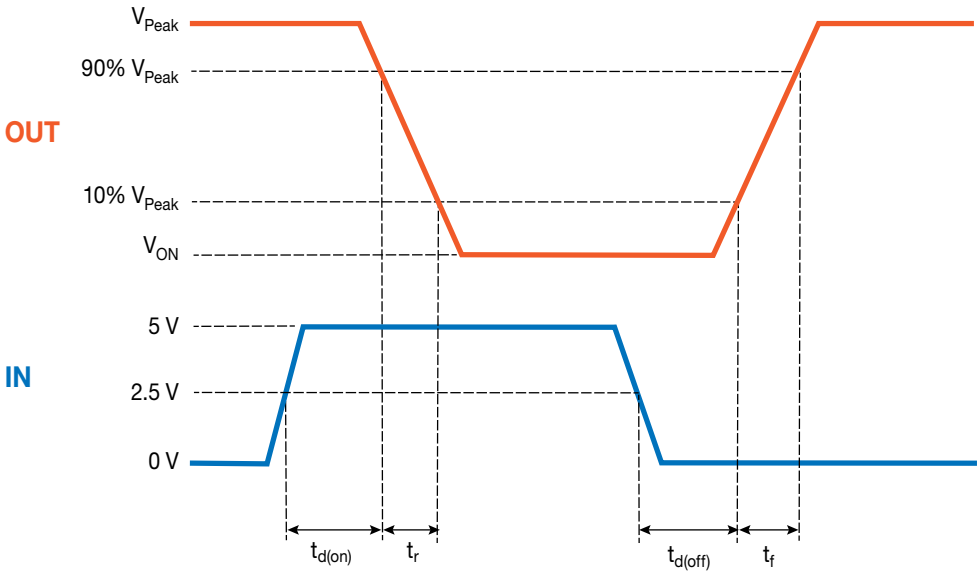
9.) V_{BIAS} levels below the UVLO- threshold result in the gate driver being disabled: The logic input to the driver is internally set to a logic low state to prevent damage to the power eGaN HEMT switch.

Switching Figures



Only pins connected during testing identified.
Pulse Generator set to 500 kHz frequency, 5% duty cycle.

Figure 1. IN-to-OUT Switching Time Test Circuit



NOTE: Waveforms exaggerated for clarity and observability.

Figure 2. IN-to-OUT Switching Time Definition

Typical Application Information

The following figures detail the suggested applications for the FBS-GAM01-P-R50 Module. For all applications, please refer to the implementation sections, following, for proper power supply bypassing and layout recommendations and criteria. In any of the following applications, if an inductive load is driven then an appropriately-rated Schottky rectifier/diode should be connected across the load to prevent destructive flyback/"kickback" voltages from destroying the FBS-GAM01-P-R50.

In all the following figures, only the pins that are considered or that require connection are identified.

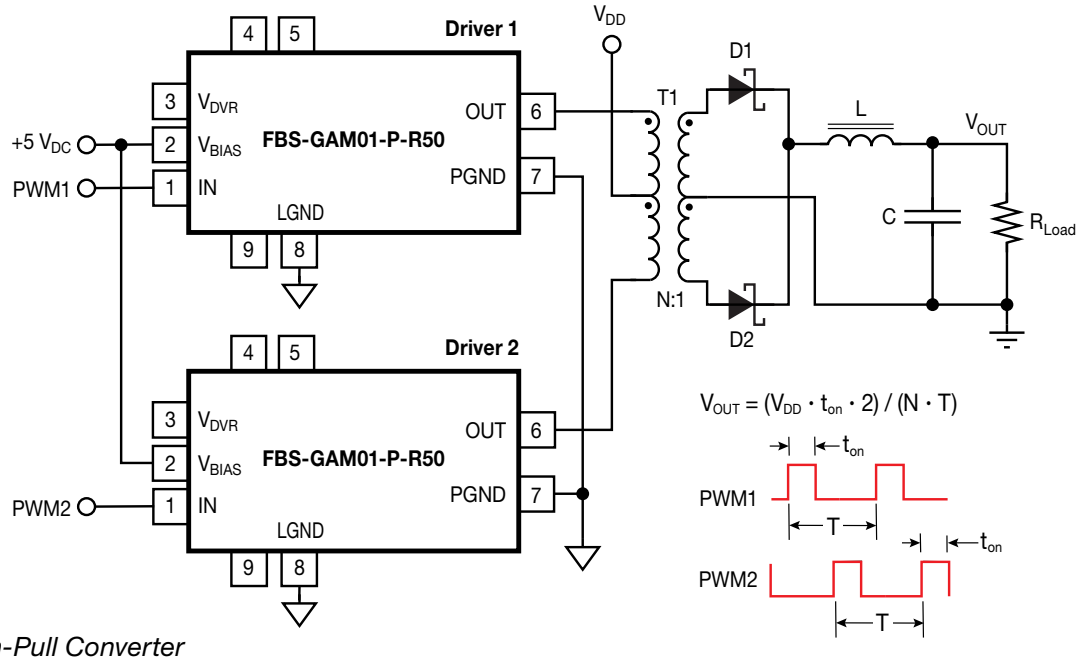


Figure 3. Push-Pull Converter

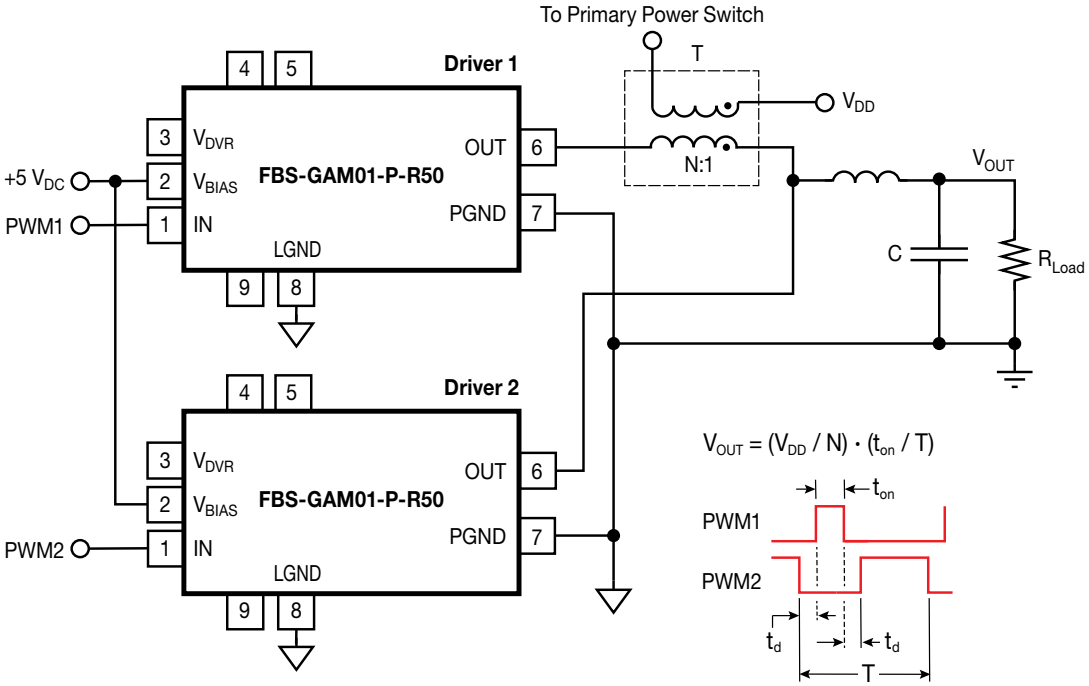
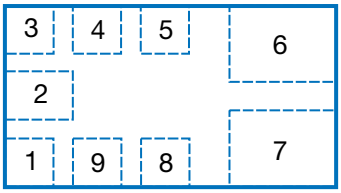


Figure 4. Synchronously-Rectified Forward Converter

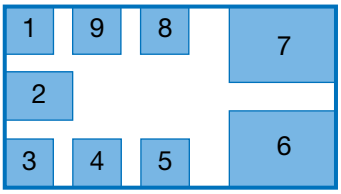
Pin Descriptions

9 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



IN (Pin 1)

The IN pin is the logic input for the gate driver. When the IN input pin is logic low ("0"), the OUT pin is in the low (~0 V_{DC}) state. When the IN pin is logic high ("1"), the OUT pin is in the ON (low impedance) state.

V_{BIAS} (Pin 2)

The V_{BIAS} pin is the raw input DC power input for the FBS-GAM01-P-R50. It is recommended that a 1.0 microfarad ceramic capacitor and a 0.1microfarad ceramic capacitor, each 25 V_{DC} rating, be connected between V_{BIAS} (pin 2) and Source Sense (pin 7) to obtain the specified switching performance.

V_{DRV} (Pin 3)

The V_{DRV} pin (Pin 3) of the FBS-GAM01-P-R50 is the protected V_{BIAS} power supply for the high-speed gate driver for the external eGaN® power HEMT. This is a test pin for the module. Unless otherwise directed in this specification, this pin should be left OPEN ("no connection") for proper operation of the module.

N/C (Pins 4 and 5)

Pins 4 and 5 are not internally connected. These internal "no connection" pins are recommended to be grounded to the system power ground/return as good engineering practice to avoid coupling unwanted noise into the internal circuitry of the FBS-GAM01-P-R50, either directly or via 0 Ω jumper resistors.

OUT (Pin 6)

The OUT pin (pin 6) is the high current output (open drain) pin of the internal power eGaN® HEMT. This is a VERY high dV/dt and dI/dt pin and the connection to the load should be as short as possible to minimize radiated EMI.

PGND (Pin 7)

The PGND pin (pin 7) is the ground return connection for the internal power circuitry in the FBS-GAM01-P- R50. This pin should be connected directly to the system power return/ground plane to minimize common source inductance, and the voltage transients associated with this inductance. If load current sensing is required, this should be accomplished via a current sense transformer in series with the OUT pin (pin 6).

LGND (Logic Ground) (Pin 8)

Logic ground for the module. For proper operation of the FBS-GAM01-P-R50, the LGND pin (Pin 7) MUST be connected directly to the system logic ground return in the application circuit.

PG/*SD (Power Good Output/Shutdown Input) (Pin 9)

The bidirectional Power Good (PG) output and Shutdown (*SD) input pin. To externally disable the FBS- GAM01-P-R50 (with the OUT pin forced to the high-impedance (OFF) state), the SD/PG pin should be connected to logic ground, such as via an open-drain/collector.
The module also incorporates a Power Good (PG) sensing circuit that disables the driver when the +5 V_{DC} gate drive bias potential (V_{BIAS}) falls below an under-voltage threshold range as specified in the Table "PG Functional Static Electrical Characteristics" (See Page 3).
During the time when the V_{BIAS} potential is below the pre-set threshold, the PG output (Pin 5) pin is pulled low (to LGND) via an open drain.
Alternatively, when the V_{BIAS} potential is above the pre-set threshold the PG pin is pulled high via an external pull up resistor to V_{DRV}.
For proper operation, pin 9 should be externally pulled-up to V_{DRV} (pin 3) with a 4.7 kΩ resistor.

DC Operation and Power Up Sequencing

The recommended power sequencing for the FBS-GAM01-P-R50 is the V_{BIAS} power supply is applied first and within the recommended operating voltage range prior to the application of V_{DD} to the circuit.

The FBS-GAM01-P-R50 is designed as a switching eGAN® HEMT driver that is inherently capable of DC (steady-state) operation. As such, there are precautions that must be observed during the application and operation of this Module. One of these precautions is power-up sequencing. The power MUST be sequenced to the circuit with V_{BIAS} being applied first and within its recommended operating voltage range before V_{DD} is applied to the circuit. This will prevent the internal gate driver output from assuming a non-deterministic state with regards to the logic input (IN) and unintentionally providing an ON drive signal to the internal eGaN® HEMT power switches when the IN pin is at logic low ("0").

Calculating FBS-GAM01 Module Power Losses and Efficiencies

The driver power losses for the FBS-GAM01 Module are determined as follows:

$$P_D(\text{Driver}) = P_{Gate}(DC) + P_{Gate}(AC) + P_{Switch}(DC) + P_{Switch}(\text{Switching}) + P_{Switch}(C_{OUT}),$$
$$\text{and } P_D(\text{Schottky}) = P_{\text{dead time}},$$

where $P_{Gate}(DC)$ are the DC gate/gate driver losses ($V_{BIAS} \cdot I_{BIAS} \cdot 0.5$), $P_{Gate}(AC)$ are the dynamic gate/gate driver losses ($P_{GD} \cdot f_s$), $P_{Switch}(DC)$ are the power switch DC losses ($I_D^2 \cdot R_{DS(on)} \cdot ton / T$), $P_{Switch}(\text{Switching})$ are the power switch losses related to the switching event [$(0.5 \cdot V_{DD} \cdot I_D \cdot tr / T) + (0.5 \cdot V_{DD} \cdot I_D \cdot t_f / T)$], $P_{Switch}(C_{OUT})$ are the losses related to switching the total drain capacitance C_{OUT} ($0.5 \cdot C_{OUT} \cdot V_{DD}^2 \cdot f_s$), and P_{dead} time are the losses related to the Schottky catch diode conduction time, which occurs during the delay "dead" time between driver switching events ($2 \cdot V_{SD} \cdot I_D \cdot t_{SD} / T$) as there are two driver switching events per period. The quantities I_{BIAS}, P_{GD}, $R_{DS(on)}$, t_r, t_f, C_{OUT} and V_{SD} may be found in the parametric tables found on pages 3 and 4, and the quantities V_{DD}, V_{BIAS}, f_s, t_{on} (the ON time of the power switch), T ($1 / f_s$) and t_{SD} are determined by the conditions of operation of the FBS-GAM01-P-R50 module.

For example, if two GAM01 drivers are operated in a synchronous rectifier application (see Figure 4), one driver will have an on time of ton and the other will have an on time of ($T - t_{on}$), and if the duty cycle is set to 50%, the power losses for the two drivers will be approximately equal. The following example calculates the losses for each driver empirically:

$$V_{DD} = 25\ V_{DC},\ I_D = 7.5\ A,\ V_{BIAS} = 5\ V_{DC},$$
$$f_s = 750\ kHz,\ T = 1/f_s = 1.33\ \mu s,\ t_{on} = 0.66\ \mu s\ (50\%\ \text{duty cycle}),\ t_{SD} = 40\ ns \text{ and } T_A = 25°C.$$

The associated losses for Driver 1 and Driver 2 are shown in the following two tables:

Table I. Driver 1 Power Loss Tabulation

GAM01 Module 1 (operating at t_{on})			
Loss	**Equation**	**Equation w/Values**	**Result**
$P_{Gate}(DC)$	$V_{BIAS} \cdot I_{BIAS}$	$5 \cdot 0.0085$	0.04 W
$P_{Gate}(AC)$	$P_{GD} \cdot f_s$	$0.021 \cdot 0.75^{(1)}$	0.02 W
$P_{Switch}(DC)$	$I_D^2 \cdot R_{DS(on)} \cdot t_{on} / T$	$7.5^2 \cdot 0.01 \cdot 0.66/1.33$	0.28 W
$P_{Switch}(\text{Switching})$	$(0.5 \cdot V_{DD} \cdot I_D \cdot t_r / T) +$ $(0.5 * V_{DD} \cdot I_D \cdot t_f / T)$	$(0.5 \cdot 25 \cdot 7.5 \cdot 0.01/1.33) +$ $(0.5 \cdot 25 \cdot 7.5 \cdot 0.012/1.33)$	1.55 W
$P_{Switch}(C_{OUT})$	$0.5 \cdot C_{OUT} \cdot V_{DD}^2 \cdot f_s$	$0.5 \cdot 1150 \cdot 10^{-12} \cdot 25^2 \cdot 750000$	0.27 W
$P_D(\text{Schottky})$	$2 \cdot V_{SD} \cdot I_D \cdot t_{SD} / T$	$2 \cdot 0.90 \cdot 7.5 \cdot 0.04/1.33$	0.41 W
P1 Total			**2.57 W**

Note: (1) 750kHz is 0.75MHz

Table II. Driver 2 Power Loss Tabulation

GAM01 Module 2 (operating at T - t_{on})			
Loss	**Equation**	**Equation w/Values**	**Result**
P_{Gate}(DC)	$V_{BIAS} \cdot I_{BIAS}$	5 · 0.0085	0.04 W
P_{Gate}(AC)	$P_{GD} \cdot f_s$	0.021 · 0.75(1)	0.02 W
P_{Switch}(DC)	$I_D^2 \cdot R_{DS(on)} \cdot t_{on} / T$	$7.5^2 \cdot 0.01 \cdot 0.66/1.33$	0.28 W
P_{Switch}(Switching)	$(0.5 \cdot V_{DD} \cdot I_D \cdot t_r / T) +$ $(0.5 * V_{DD} \cdot I_D \cdot t_f / T)$	$(0.5 \cdot 25 \cdot 7.5 \cdot 0.01/1.33) +$ $(0.5 \cdot 25 \cdot 7.5 \cdot 0.012/1.33)$	1.55 W
$P_{Switch}(C_{OUT})$	$0.5 \cdot C_{OUT} \cdot V_{DD}^2 \cdot f_s$	$0.5 \cdot 1150 \cdot 10^{-12} \cdot 25^2 \cdot 750000$	0.27 W
P_D(Schottky)	$2 \cdot V_{SD} \cdot I_D \cdot t_{SD} / T$	2 · 0.90 · 7.5 · 0.04/1.33	0.41 W
P2 Total			**2.57 W**

Note: (1) 750 kHz is 0.75MHz

The total module loss for GAM01 Module 1 is P1(TOTAL) = 2.57 W and the total module loss for GAM01 Module 2 is P2 (TOTAL) = 2.57 W. The power delivered to the load is $V_{DD} \cdot I_D \cdot t_{on} / T$, or 93.8 W. The conversion efficiency for the two GAM01 modules, η, is $P_{LOAD} / (P_{LOAD} + P_{LOSS})$ = 93.8 / 99.1 = 94.7%.

It is clear in the previous power loss/efficiency example that the majority of the losses experienced by the GAM01 are related to dynamic (switching) losses. Thus, to achieve the lowest losses and highest possible efficiency, it is desirable to operate the synchronously-rectified circuit with the lowest possible V_{DD} potential.

Recommended V_{DD}-to-PGND Power Supply Bypassing

The V_{DD} power supply associated with the high current output (OUT, pin 6) of the FBS-GAM01-P-R50 requires proper high frequency bypassing to PGND (pin 7) in-order to prevent harmful switching noise-related spikes from degrading or damaging the internal circuitry in the FBS-GAM01-P-R50 module, or impacting operating performance. It is recommended that a minimum of two (2) 4.7 microfarad ceramic capacitors, one (1) 1.0 microfarad ceramic capacitor and one (1) 0.1 microfarad ceramic capacitor, all with 100 V_{DC} ratings, be connected from V_{DD} to PGND. All four of these capacitors should be low ESR types, if possible. It is strongly recommended that these capacitors inscribe the smallest possible loop area between V_{DD} and PGND so-as to minimize the inductance, and thus voltage transients, related to this loop area. Regardless, different end-use implementations will require different V_{DD} bypass capacitor placements, and it is strongly recommended that the chosen bypassing scheme be evaluated for its effectiveness.

Suggested FBS-GAM01-P-R50 Schematic Symbol

The suggested schematic symbol for the FBS-GAM01-P-R50 is shown in Figure 5. This symbol groups the I/O pins of the FBS-GAM01-P-R50 into groups of similar functionalities.

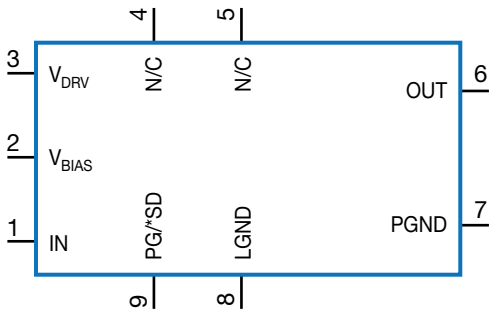


Figure 5. Suggested FBS-GAM01-P-R50 Schematic Symbol

Radiation Characteristics

The **FBS-GAM01-P-R50** is a Radiation Hardness-Assured 50 V_{DC}/12 A Single Low-Side Power Driver Module.

- EPC Space's FBS-GAM01-P-R50 internally utilizes eGaN HEMT technology designed, fabricated and tested per Mil-Std-750 Method 1019 for total ionizing dose validation with total ionizing with an in-situ Gamma Bias for (i) V_{GS} = 5V, (ii) V_{DS} = V_{GS} = 0 V and (iii) V_{DS} = 80% B_{VDSS}.
- Under the above prescribed conditions EPC Space can guarantee parametric data limits as outlined within the **FBS-GAM01-P-R50** datasheet with the additional pre/post radiation effects guarantee under a best practice commercial screened reliability level in an Epoxy Over-Mold non-hermetic package outline.

When incorporating EPC Space radiation validated/assured HEMT materials, the **FBS-GAM01-P-R50** series are "guaranteed by designed" to survive High Dose Rate TID to levels of 100 kRad (Si) with Single Event Immunity to:

Heavy Ion: Au, LET (Si)= 83.7, 2482 MeV, Range = 130 µm -- **Up to 100 V_{DS} Voltage Maximum**.

Thermal Characteristics

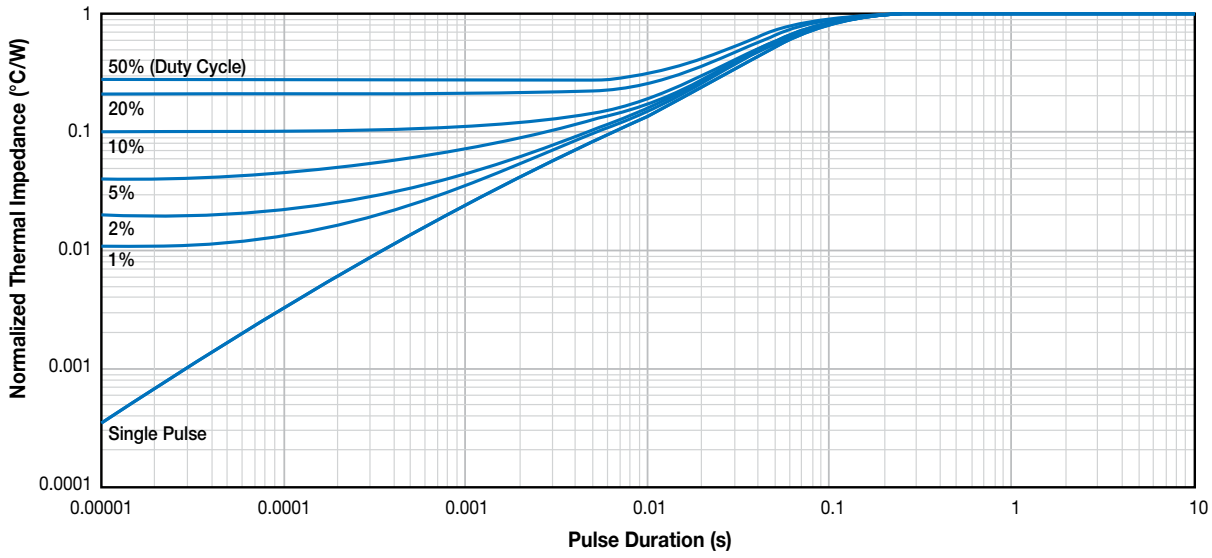


Figure 6. Typical Power eGAN® HEMT Normalized Junction-to-Case Thermal Impedance

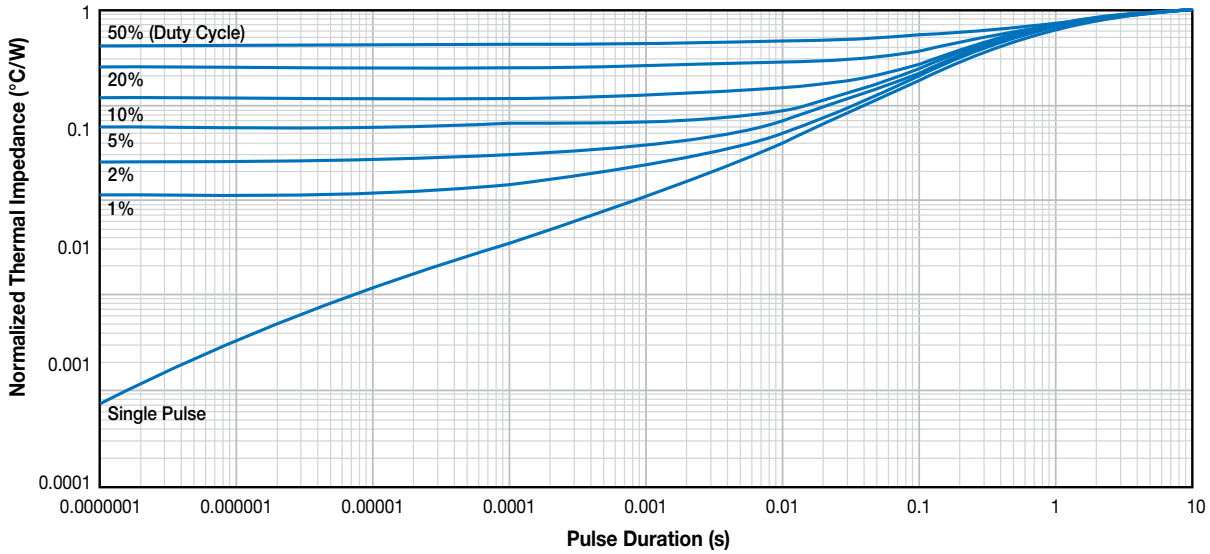
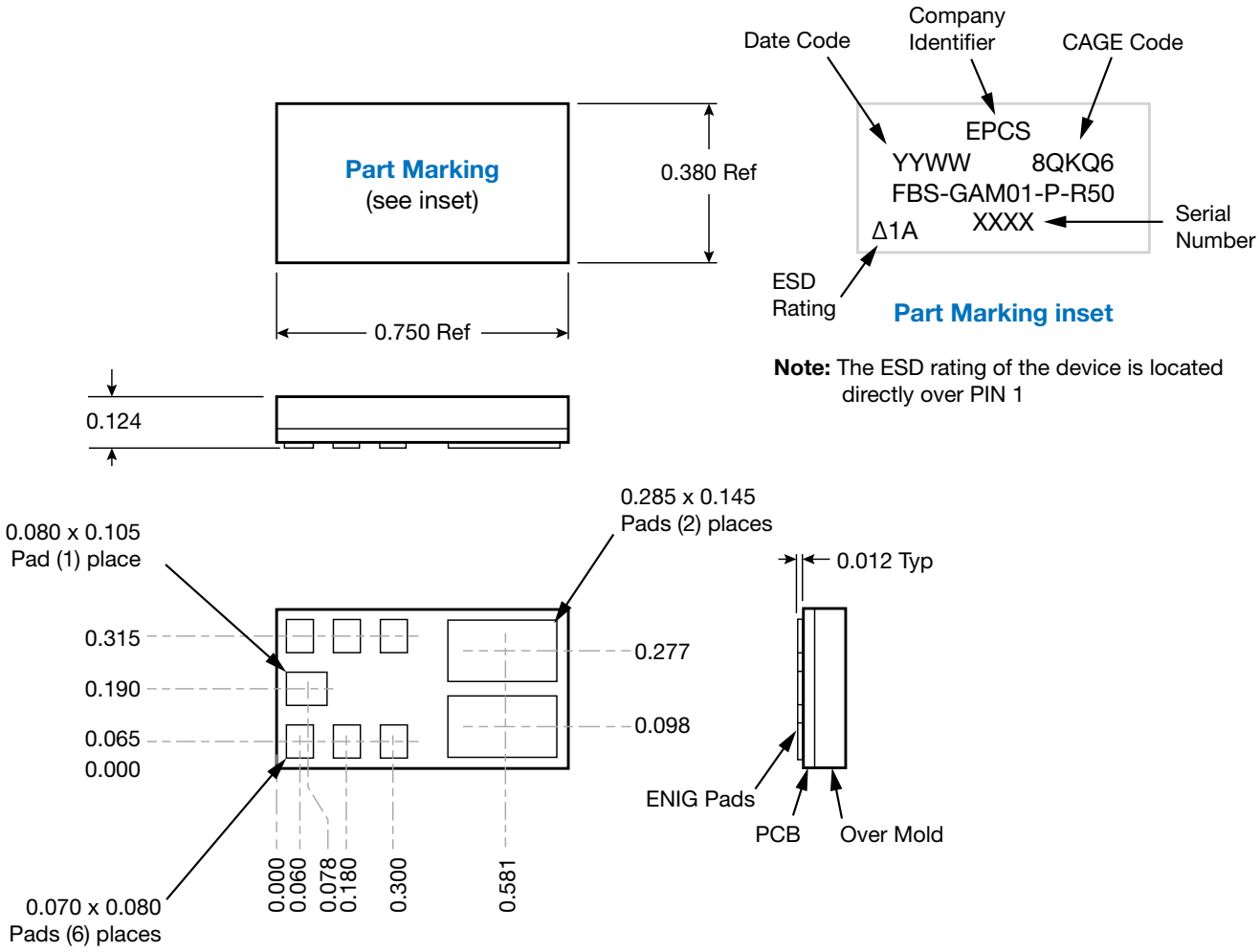


Figure 7. Typical Catch Schottky Normalized Junction-to-Case Thermal Impedance

Package Outline, Dimensions, and Part Marking



Note: All dimensions are in inches
ALL tolerances +/- 0.010

Figure 8. FBS-GAM01-P-R50 Package Outline and Dimensions

Recommended PCB Solder Pad Configuration

The novel I/O "pillar" pads fabricated onto the bottom surface of the FBS-GAM01-P-R50 module are designed to provide optimal electrical, thermal and mechanical properties for the end-use system designer. To achieve the full benefit of these properties, it is important that the FBS-GAM01-P-R50 module be soldered to the PCB motherboard using SN63 (or equivalent) solder. Care should be taken during processing to insure there is minimal solder voiding in the contacts to the OUT (pin 6) and PGND (pin 7) pads on the module, as these are high current connections. The recommended pad dimensions and locations are shown in Figure 9. All dimensions are shown in inches.

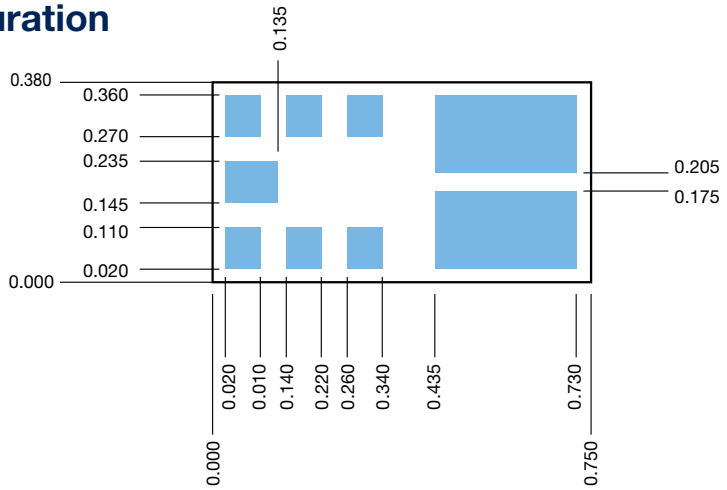


Figure 9. Recommended PCB Solder Pad Configuration (Bottom View)

Sn63/Pb37 No Clean Solder Paste Typical Example Profile

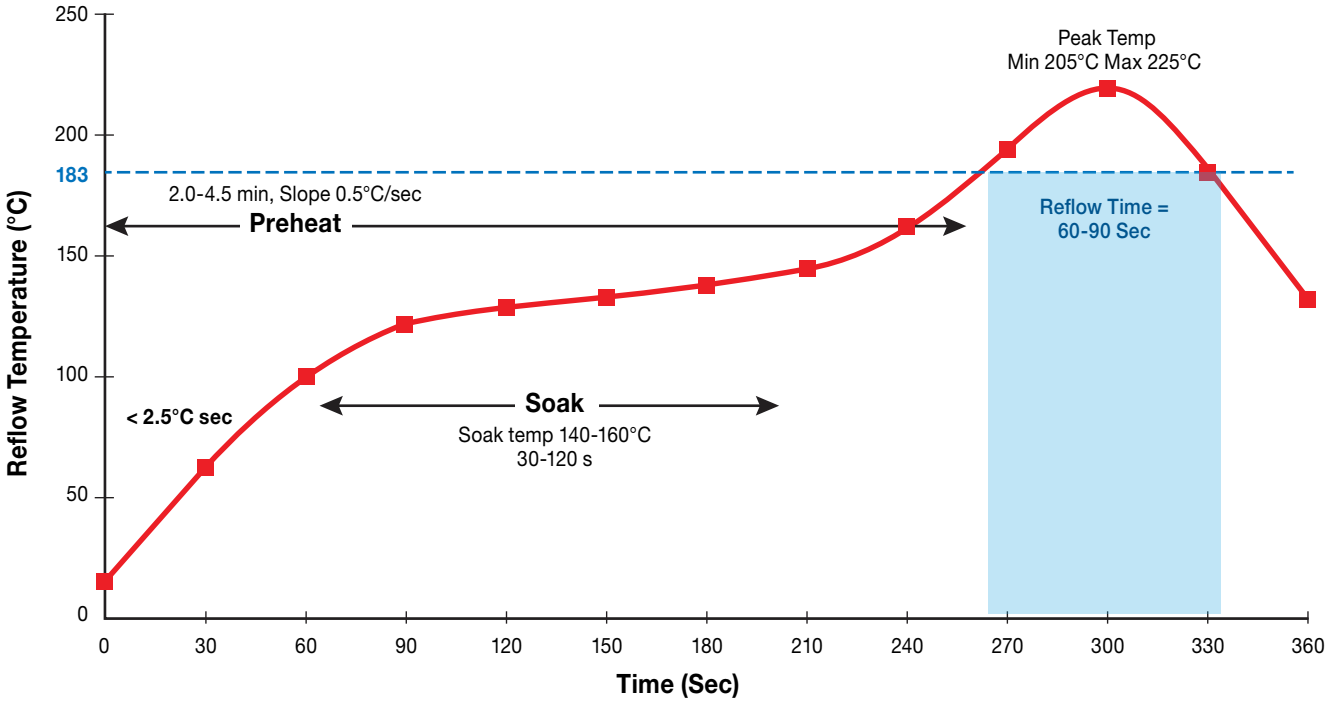


Figure 10. Typical GAM01 Solder Reflow Profile

Preheat Zone – The preheat zone, is also referred to as the ramp zone, and is used to elevate the temperature of the PCB to the desired soak temperature. In the preheat zone the temperature of the PCB is constantly rising, at a rate that should not exceed 2.5°C/sec. The oven's preheat zone should normally occupy 25-33% of the total heated tunnel length.

The Soak Zone – normally occupies 33-50% of the total heated tunnel length exposes the PCB to a relatively steady temperature that will allow the components of different mass to be uniform in temperature. The soak zone also allows the flux to concentrate and the volatiles to escape from the paste.

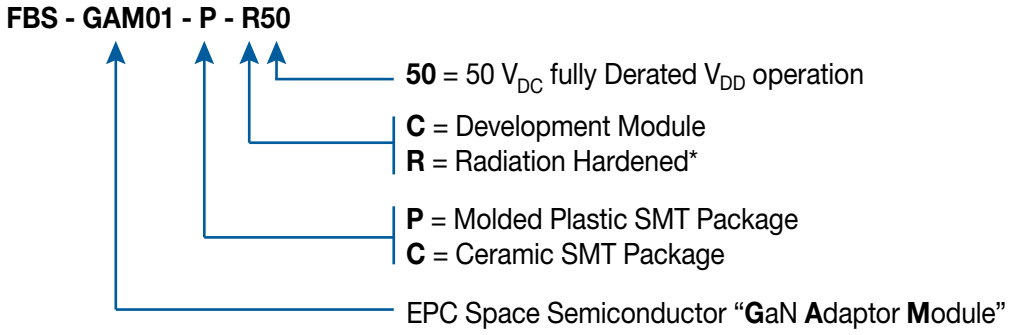
The Reflow Zone – or spike zone is to elevate the temperature of the PCB assembly from the activation temperature to the recommended peak temperature. The activation temperature is always somewhat below the melting point of the alloy, while the peak temperature is always above the melting point.

Reflow – Best results achieved when reflowed in a forced air convection oven with a minimum of 8 zones (top & bottom), however reflow is possible with a four-zone oven (top & bottom) with the recommended profile for a forced air convection reflow process. The melting temperature of the solder, the heat resistance of the components, and the characteristics of the PCB (i.e. density, thickness, etc.) determine the actual reflow profile.

Note: FBS-GAM01-P-R50 solder attachment has a maximum peak 230°C dwell temperature limit, exceeding the maximum peak temperature can cause damage the unit.

Reflow Process Disclaimer – The profile is as stated "Example." The-end user can optimize reflow profiling based against the actual solder paste and reflow oven used. EPC Space assumes no liability in conjunction with the use of this profile information.

EPC Space Part Number Information



*FBS-GAM01-P-R50 (Utilizes High Lead Content Die) and
FBS-GAM01-C-R50 (Utilizes High Lead Content Die)

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Revisions

Datasheet Revision	Product Status
REV -	Proposal/development
M-702-007-Q6	Characterization and Qualification
	Production Released

Information subject to change without notice.
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