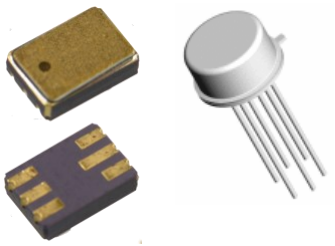
2N4854, 2N4854U

NPN/PNP Dual Silicon Transistors

Rev. V1

Features

- Available in JAN, JANTX and JANTXV per MIL-PRF-19500/421
- Unitized, Dual Transistors
- Electrically Isolated, Complimentary NPN and PNP
- TO-78 and U package types



Electrical Characteristics (T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Breakdown Voltage	I_C = 10 mA dc	$V_{(BR)CEO}$	V dc	40	—
Collector - Base Cutoff Current	V_{CB} = 60 V dc V_{CB} = 50 V dc	I_{CBO1} I_{CBO2}	µA dc nA dc	—	10 10
Emitter - Base Cutoff Current	V_{EB} = 5.0 V dc V_{EB} = 3.0 V dc	I_{EBO1} I_{EBO2}	µA dc nA dc	—	10 10
Forward Current Transfer Ratio	V_{CE} = 1.0 V dc; I_C = 150 mA dc V_{CE} = 10 V dc; I_C = 100 µA dc V_{CE} = 10 V dc; I_C = 1.0 mA dc V_{CE} = 10 V dc; I_C = 10 mA dc V_{CE} = 10 V dc; I_C = 150 mA dc V_{CE} = 10 V dc; I_C = 300 mA dc	h_{FE1} h_{FE2} h_{FE3} h_{FE4} h_{FE5} h_{FE6}	h_{FE}	50 35 50 75 100 35	300
Collector - Emitter Saturation Voltage	I_B = 15 mA dc; I_C = 150 mA dc	$V_{CE(SAT)}$	Vdc	—	0.40
Base - Emitter Saturation Voltage	I_B = 15 mA dc; I_C = 150 mA dc	$V_{BE(SAT)}$	Vdc	0.8	1.25

Electrical Characteristics (T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Small-Signal Short-Circuit Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 1 mA dc; f = 1 kHz	h_{fe}	—	60	300
Small-Signal Common Emitter Input Impedance	V_{CE} = 10 V dc; I_C = 1 mA dc; f = 1 kHz	h_{ie}	kΩ	1.5	9
Small-Signal Common Emitter Output Admittance	V_{CE} = 10 V dc; I_C = 1 mA dc; f = 1 kHz	h_{oe}	µhmo	—	50
Collector-Base Cutoff Current	T_A = +150°C V_{CB} = 50 V dc	I_{CBO3}	µA dc	—	10
Forward Current Transfer Ratio	T_A = -55°C V_{CE} = 10 V dc; I_C = 10 mA dc	h_{FE7}	—	12	—
Magnitude of Small-Signal Short-Circuit Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 20 mA dc; f = 100 MHz	$\lvert h_{fe} \rvert$	—	2.0	10
Open Circuit Output Capacitance	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}	pF	—	8.0
Noise Figure	V_{CE} = 10 V dc; I_C = 100 µA dc; f = 1kHz; R_G = 1 kΩ	NF	—	8	dB
Collector Emitter Nonlatching Voltage	See figure 10	V_{CE}	V dc	40	—
Switching Characteristics					
Turn-On Time (saturated)	See figure 7	t_{on}	ns	—	45
Turn-Off Time (saturated)	See figure 8	t_{off}	ns	—	300
Pulse Response	See figure 9	$t_{on} + t_{off}$	ns	—	18

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Absolute Maximum Ratings (T_A = +25°C unless otherwise specified)

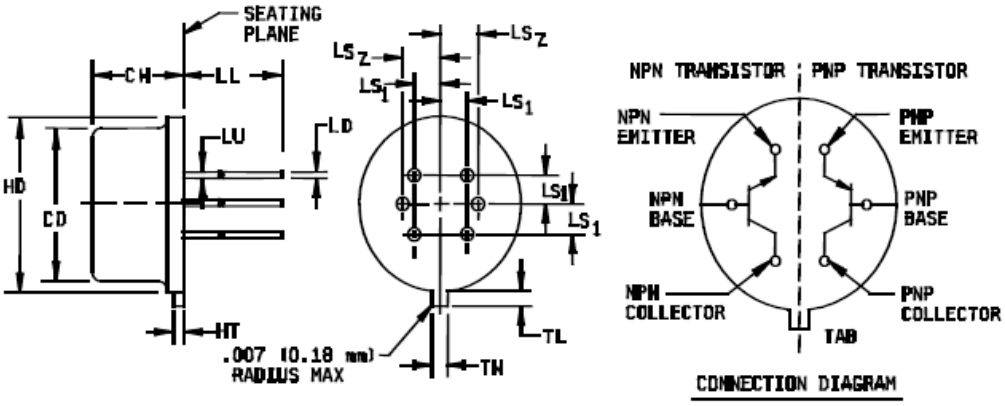
Ratings	Symbol	Value
Collector - Emitter Voltage	V_{CEO}	40 V dc
Collector - Base Voltage	V_{CBO}	60 V dc
Emitter - Base Voltage	V_{EBO}	5.0 V dc
Collector Current	I_C	600 mA dc
Total Power Dissipation @ T_A = +25°C One Transistor Total Device	P_T	 0.30 W (4) 0.60 W (4)
Total Power Dissipation @ T_C = +25°C One Transistor Total Device	P_T (1)	 1.0 W (5) 2.0 W (5)
Operating & Storage Temperature Range	T_J, T_{STG}	-65°C to +200°C
$V_{1C—2C}$	V dc	±120
Lead To Case Voltage	V dc	±120

Thermal Characteristics

Types	$R_{\theta JA}$ One Transistor	$R_{\theta JA}$ Total Device	$R_{\theta JSP}$ One Section	$R_{\theta JSP}$ Both Sections
	°C/W	°C/W	°C/W	°C/W
2N4854	350	290		
2N4854U			110 (6)	90 (6)

(1) T_C rating does not apply to surface mount devices (2N4854U).
(2) For T_A > +25°C, derate linearly 1.43 mW/°C one transistor, 2.00 mW/°C both transistors.
(3) For T_C > +25°C, derate linearly 4.0 mW/°C one transistor, 8.0 mW/°C both transistors.
(4) For T_A > +25°C, derate linearly 1.71 mW/°C one transistor, 3.43 mW/°C both transistors
(5) For T_C > +25°C, derate linearly 5.71 mW/°C one transistor, 11.43 mW/°C both transistors.
(6) For U package the thermal resistance is $R_{\theta SP}$.

Outline Drawing (TO-78)



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.140	.260	3.56	6.60	
HD	.335	.370	8.51	9.40	
HT	.009	.125	0.23	3.18	
LD	.016	.021	0.41	0.53	3, 7
LL	.500	1.750	12.70	44.45	7

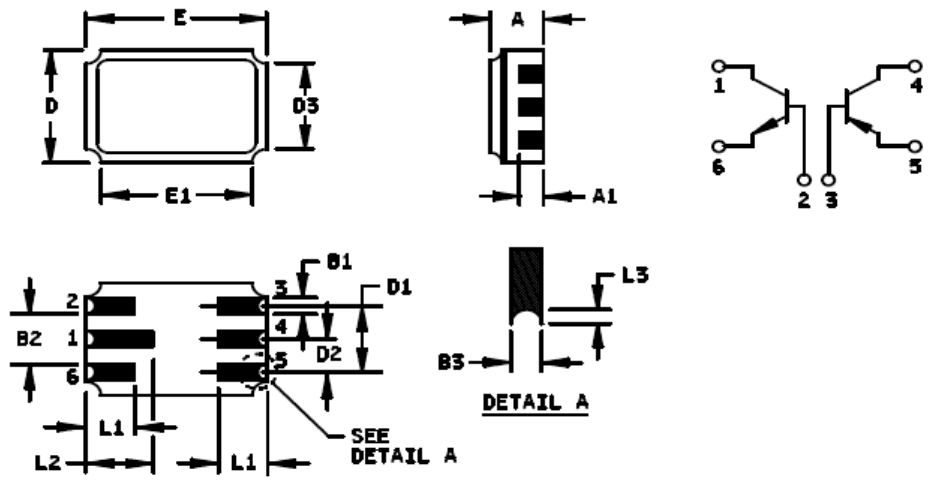
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
LS1	.0707 Nom.		1.796 Nom.		5
LS2	.1000 Nom.		2.540 Nom.		5
LU	.016	.019	0.41	0.48	4, 7
TL	.029	.045	0.74	1.14	6
TW	.028	.034	0.71	0.86	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Measured in the zone beyond .250 inch (6.35 mm) from the seating plane.
4. Measured in the zone .050 inch (1.27 mm) and .250 inch (6.35 mm) from the seating plane.
5. When measured in a gauging plane .054 +.001, -.000 inch (1.37 +0.03, -0.00 mm) below the seating plane of the transistor, maximum diameter leads shall be within .007 inch (0.18 mm) of their true location relative to a maximum width tab. Smaller diameter leads shall fall within the outline of the maximum diameter lead tolerance.
6. Measured from the maximum diameter of the actual device.
7. All six leads.
8. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions of transistor type 2N4854 (all quality levels, similar to TO-78).

Outline Drawing (U)



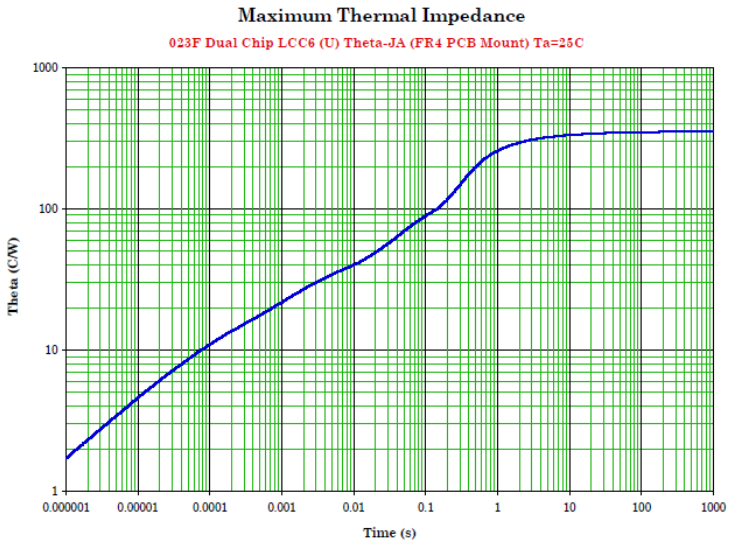
Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.058	.100	1.47	2.54
A_1	.026	.039	0.66	0.99
B_1	.022	.028	0.56	0.71
B_2	.072 Ref.		1.83 Ref.	
B_3	.006	.022	0.15	0.56
D	.165	.175	4.19	4.45
D_1	.095	.105	2.41	2.67

Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
D_2	.045	.055	1.14	1.40
D_3		.175		4.45
E	.240	.250	6.10	6.35
E_1		.250		6.35
L_1	.060	.070	1.52	1.78
L_2	.082	.098	2.08	2.49
L_3	.003	.007	0.08	0.18

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15 mm) for solder dipped leadless chip carriers.

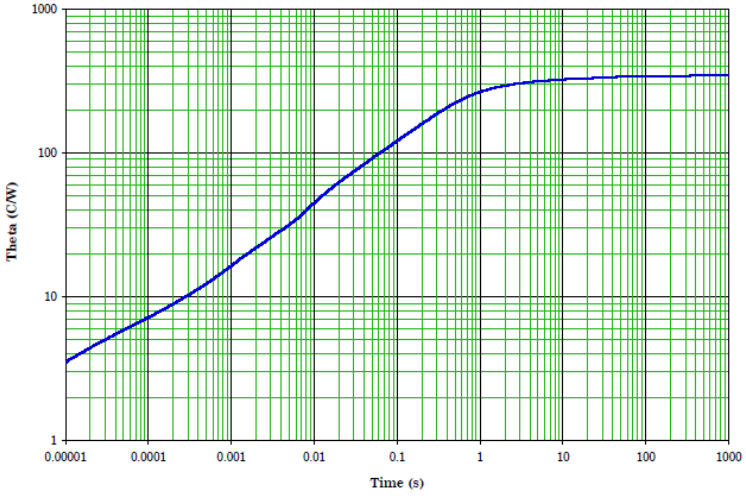
FIGURE 3. Physical dimensions of transistor type 2N4854U.

Graphs



Thermal resistance = 350°C/W one side, 290°C/W both sides operating in "parallel".
Ta = 25°C (PCB FR4 Mounted).

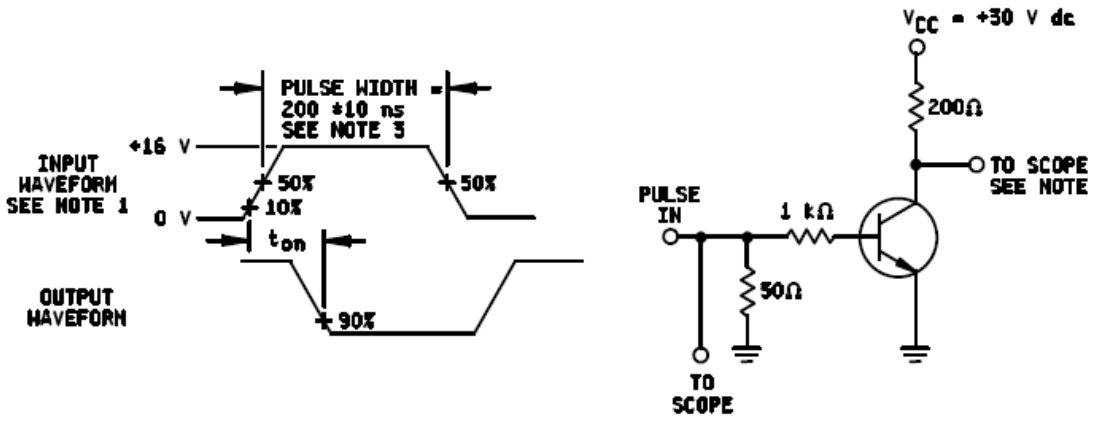
FIGURE 5. Thermal impedance graph ($R_{\theta JPCB}$) for 2N4854U (U).



Thermal impedance TO-78 package dual 023F chips,
Thermal resistance = 350°C/W one side, 290°C/W both sides operating in "parallel".
T_A = 25°C (air cooled).

FIGURE 6. Thermal impedance graph ($R_{\theta JA}$) for 2N4854 (all quality levels, similar to TO-78).

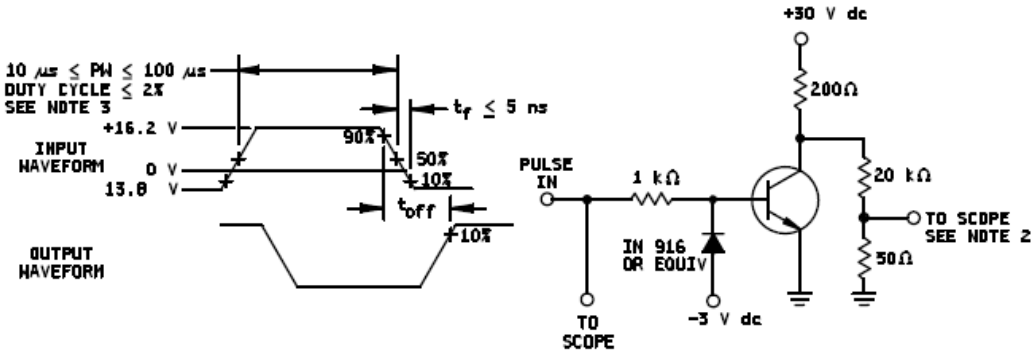
Test Circuits



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50 Ω.
2. Sampling oscilloscope: Z_{IN} ≥ 100 kΩ, C_{IN} ≤ 12 pF, rise time ≤ 0.2 ns.
3. The signs, polarity symbols, and waveforms shown are for the NPN transistor; the signs and polarity symbols are reversed for the PNP triode (see 1.2 herein).

FIGURE 7. Saturated turn-on switching time test circuit.

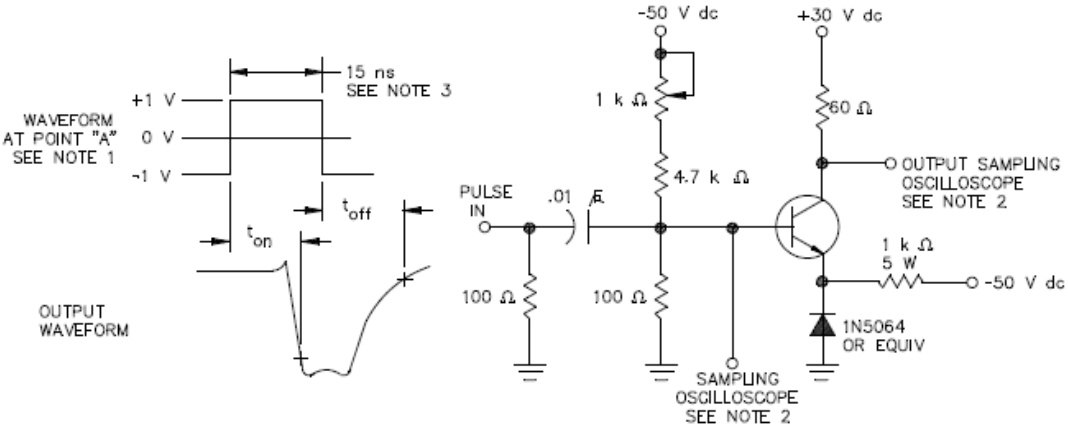


NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50 Ω.
2. Sampling oscilloscope: Z_{IN} ≥ 100 kΩ, C_{IN} ≤ 12 pF, rise time ≤ 0.2 ns.
3. The signs, polarity symbols, and waveforms shown are for the NPN transistor; the signs and polarity symbols are reversed for the PNP triode (see 1.2 herein).

FIGURE 8. Saturated turn-off switching time test circuit.

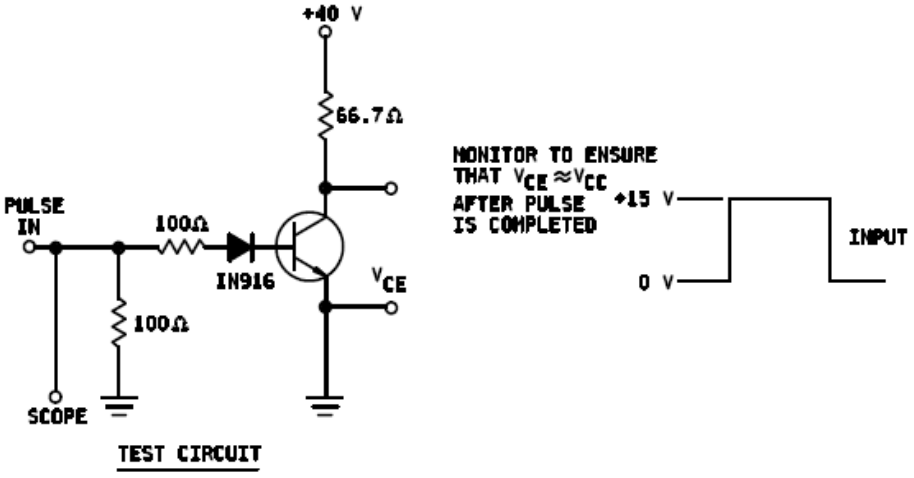
Test Circuits



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50 Ω.
2. Sampling oscilloscope: Z_{IN} ≥ 100 kΩ, C_{IN} ≤ 12 pF, rise time ≤ 0.2 ns.
3. The signs, polarity symbols, and waveforms shown are for the NPN transistor; the signs and polarity symbols are reversed for the PNP triode (see 1.2 herein).

FIGURE 9. Nonsaturated switching time test circuit.



NOTE: The input waveform has the following characteristics: PW ≤ 10 μs, duty cycle ≤ 2 percent.

FIGURE 10. Collector emitter nonlatching voltage test circuit.