2N4029, 2N4033, 2N4033UA, 2N4033UB

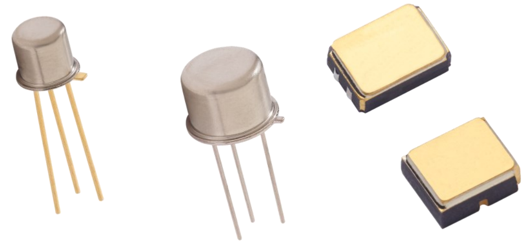
VPT COMPONENTS

PNP Silicon Transistor

Rev. V2

Features

- Available in JAN, JANTX, JANTXV and JANS per MIL-PRF-19500/512
- 2N4029 available in TO-18
- 2N4033 available in TO-39, UA and UB package styles
- Suitable for High Speed Switching and Driver Applications



Electrical Characteristics

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Off Characteristics					
Collector - Base Cutoff Current	V_{CB} = -80 V dc	I_{CBO1}	μA dc	—	-10
Emitter - Base Cutoff Current	V_{EB} = -5 V dc	I_{EBO1}	μA dc	—	-10
Collector - Base Cutoff Current	V_{CB} = -60V dc	I_{CBO2}	nA dc	—	-10
Collector - Emitter Cutoff Current	V_{BE} = -2.0 V dc; V_{CE} = -60V dc	I_{CEX1}	nA dc	—	-25
Base - Emitter Cutoff Current	V_{BE} = -3.0 V dc	I_{EBO2}	nA dc	—	-25
Collector-Base Cutoff Current	T_A = +150°C V_{CB} = -60 V dc	I_{CBO3}	μA dc	—	-25
On Characteristics					
Forward Current Transfer Ratio	V_{CE} = -5.0 V dc; I_C = -100 μA dc V_{CE} = -5.0 V dc; I_C = -100 mA dc V_{CE} = -5.0 V dc; I_C = -500 mA dc V_{CE} = -5.0 V dc; I_C = -1.0 A dc	h_{FE1} h_{FE2} h_{FE3} h_{FE4}	-	50 100 70 25	300
Collector - Emitter Saturated Voltage	I_C = -150 mA dc; I_B = -15 mA dc I_C = -500 mA dc; I_B = -50 mA dc I_C = -1.0 A dc; I_B = -100 mA dc	$V_{CE(SAT)1}$ $V_{CE(SAT)2}$ $V_{CE(SAT)3}$	V dc	—	-0.15 -0.50 -1.0
Base - Emitter Saturated Voltage	I_C = -150 mA dc; I_B = -15 mA dc I_C = -500 mA dc; I_B = -50 mA dc	$V_{BE(SAT)1}$ $V_{BE(SAT)2}$	V dc	—	-0.9 -1.2
Forward Current Transfer Ratio	T_A = -55°C V_{CE} = -5.0 V dc; I_C = -500 mA dc	h_{FE5}	-	30	

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Parameter	Test Conditions	Symbol	Units	Min.	Max.
Dynamic Characteristics					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio	V_{CE} = -10 V dc; I_C = -50 mA dc; f = 100 MHz	$\|h_{FE}\|$	-	1.5	6.0
Open Circuit Output Capacitance	V_{CB} = -10 V dc; I_E = 0; 100 kHz $\leq f \leq$ 1 MHz	C_{obo}	pF	—	20
Input Capacitance (Output Open-Circuited)	V_{EB} = -0.5 V dc; I_C = 0; 100 kHz $\leq f \leq$ 1 MHz	C_{ibo}	pF	—	80
Pulse Response					
On-Time	I_C = -500 mA dc; I_{B1} = -50 mA dc	td	ns	—	15
Rise Time	I_C = -500 mA dc; I_{B1} = -50 mA dc	tr	ns	—	25
Storage Time	I_C = -500 mA dc; I_{B1} = -50 mA dc	ts	ns	—	175
Fall Time	I_C = -500 mA dc; I_{B1} = -50 mA dc	tf	ns	—	35

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Absolute Maximum Ratings (T_A = +25°C unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage	V_{CEO}	-80 V dc
Collector - Base Voltage	V_{CBO}	-80 V dc
Emitter - Base Voltage	V_{EBO}	-5.0 V dc
Collector Current	I_C	-1.0 A dc
Total Power Dissipation T_A = +25°C (1) (2) 2N4033 2N4029 2N4033UA 2N4033UB	P_T	 0.800 W 0.500 W 0.500 W 0.500 W (4)
Total Power Dissipation T_C = +25°C (1) (2) 2N4033 2N4029 2N4033UA 2N4033UB	P_T	 4 W 1 W N/A N/A
Total Power Dissipation $T_{SP(IS)}$ = +25°C (1) (2) 2N4033 2N4029 2N4033UA 2N4033UB	P_T	 N/A N/A 1.5 W 1.5 W
Junction & Storage Temperature Range	T_J, T_{STG}	-65°C to +200°C

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Absolute Maximum Ratings (T_A = +25°C unless otherwise specified)

Ratings	Symbol	Value
Thermal Resistance, Junction to Ambient [2] [3] 2N4033 2N4029 2N4033UA 2N4033UB	$R_{\theta JA}$	195 °C/W 325 °C/W 325 °C/W 325 °C/W
Thermal Resistance, Junction to Case [2] [3] 2N4033 2N4029 2N4033UA 2N4033UB	$R_{\theta JC}$	40 °C/W 150 °C/W N/A N/A
Thermal Resistance, Junction to Case Kovar [2] [3] 2N4033 2N4029 2N4033UA 2N4033UB	$R_{\theta JC}$	35 °C/W N/A N/A N/A
Thermal Resistance, Junction to Solder Pad, Infinite Sink[2] [3] 2N4033 2N4029 2N4033UA 2N4033UB	$R_{\theta JSP(IS)}$	N/A N/A 110 °C/W 90 °C/W
Thermal Resistance, Junction to Solder Pad, Ambient[2] [3] 2N4033 2N4029 2N4033UA 2N4033UB	$R_{\theta JSP(AM)}$	N/A N/A 40 °C/W N/A

(1) For derating, for encapsulated devices, see figures 7, 8, 9, 10 and 11 of MIL-PRF-19500/512
(2) See paragraph 3.3 of MIL-PRF-19500/512
(3) For thermal impedance curves, see figures 12, 13, 13a, 14, 15, 16, 17 and 18 of MIL-PRF-19500/512
(4) For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute figures 8 and 16 for the UB package and use $R_{\theta JA}$

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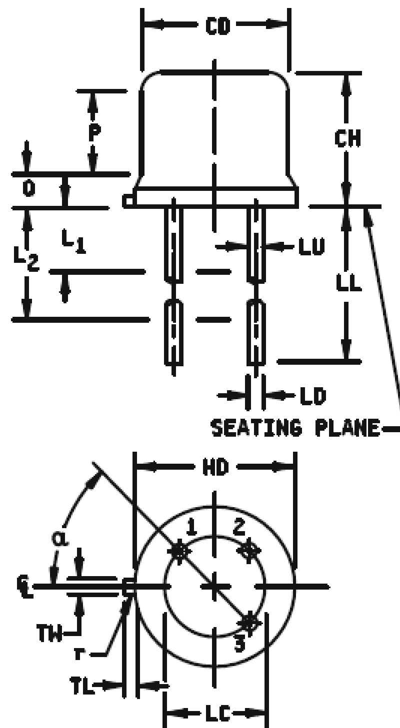
Outline Drawing (TO-18)

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7, 8
LL	.500	.750	12.70	19.05	7, 8, 12
LU	.016	.019	0.41	0.48	7, 8
L_1		.050		1.27	7. 8
L_2	.250		6.35		7, 8
Q		.040		1.02	5
TL	.028	.048	0.71	1.22	3, 4
TW	.036	.046	0.91	1.17	3
R		.010		0.25	10
P	.100		2.54		
α	45°TP		45°TP		6



NOTES:

1. Dimensions are in inches.
2. Millimeters equivalents are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 –0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
12. For "L" suffix devices, dimension LL is 1.50 (38.10 mm) minimum, 1.75 (44.45 mm) maximum.

FIGURE 1. Physical dimensions (type 2N4029) (TO-18).

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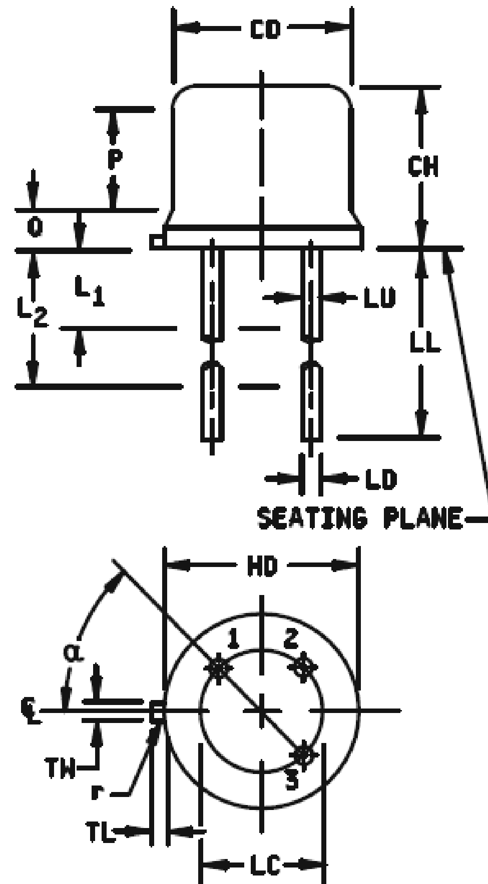
Outline Drawing (TO-39)

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7, 8
LL	.500	.750	12.70	19.05	7, 8, 12
LU	.016	.019	0.41	0.48	7, 8
L_1		.050		1.27	7, 8
L_2	.250		6.35		7, 8
Q		.050		1.27	5
TL	.029	.045	0.74	1.14	3, 4
TW	.028	.034	0.71	0.86	3
R		.010		0.25	10
P	.100		2.54		
α	45°TP		45°TP		6



NOTES:
1. Dimensions are in inches.
2. Millimeters equivalents are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
12. For "L" suffix devices, dimension LL is 1.50 (38.10 mm) minimum, 1.75 (44.45 mm) maximum.

FIGURE 2. Physical dimensions (type 2N4033) (TO-39).

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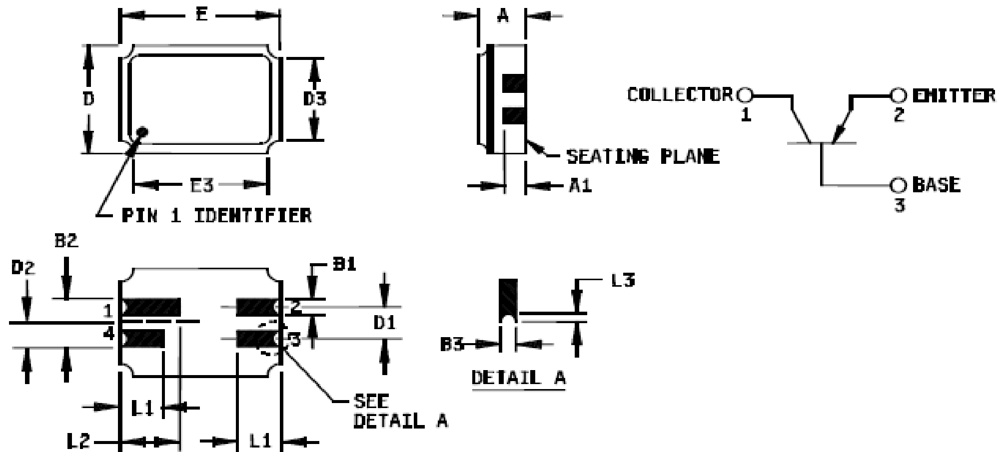
Outline Drawing (UA Package)



Ltr	Dimensions				Notes	Ltr	Dimensions				Notes
	Inches		Millimeters				Inches		Millimeter		
	Min	Max	Min	Max			Min	Max	Min	Max	
A	.061	.075	1.55	1.91	3	D_2	.0375 BSC		0.952 BSC		
A_1	.029	.041	0.74	1.04		D_3		.155		3.94	
B_1	.022	.028	0.56	0.71		E	.215	.225	5.46	5.72	
B_2	.075 REF		1.91 REF			E_3		.225		5.72	
B_3	.006	.022	0.15	0.56	5	L_1	.032	.048	0.81	1.22	
D	.145	.155	3.68	3.9		L_2	.072	.088	1.83	2.24	
D_1	.045	.055	1.14	1.39		L_3	.003		0.08		5

NOTES:

1. Dimensions are in inches.
2. Millimeters equivalents are given for general information only.
3. Dimension “A” controls the overall package thickness. When a window lid is used, dimension “A” must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
5. Dimensions “B3” minimum and “L3” minimum and the appropriately castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension “B3” maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.

FIGURE 3. Physical dimensions, surface mount (UA version).

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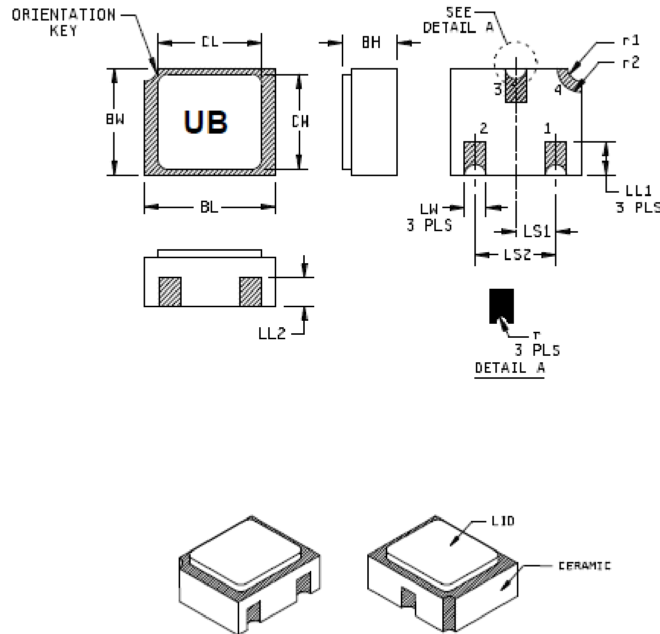
Outline Drawing (UB Package)



Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.97	
LL2	.017	.035	0.43	0.89	

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LS_1	.036	.040	0.91	1.02	
LS_2	.071	.079	1.80	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

FIGURE 4. Physical dimensions, surface mount (UB version).

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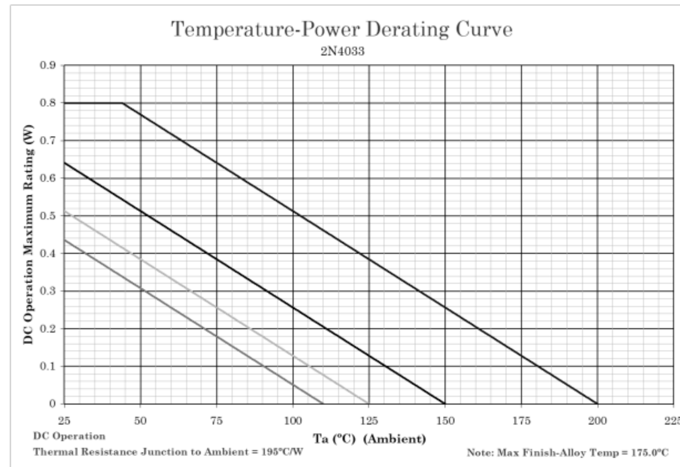
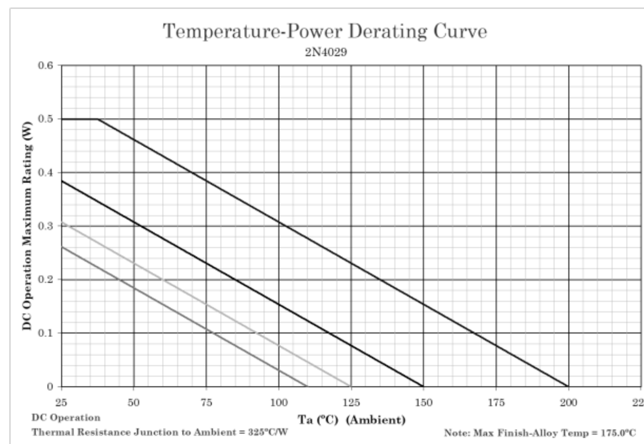
Temperature-Power Derating Curves



NOTES:
1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 7. Derating for 2N4033 ($R_{\theta JA}$) (TO-39).



NOTES:
1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8. Derating for 2N4029 ($R_{\theta JA}$) (TO-18), leads .125 inch (3.17 mm).

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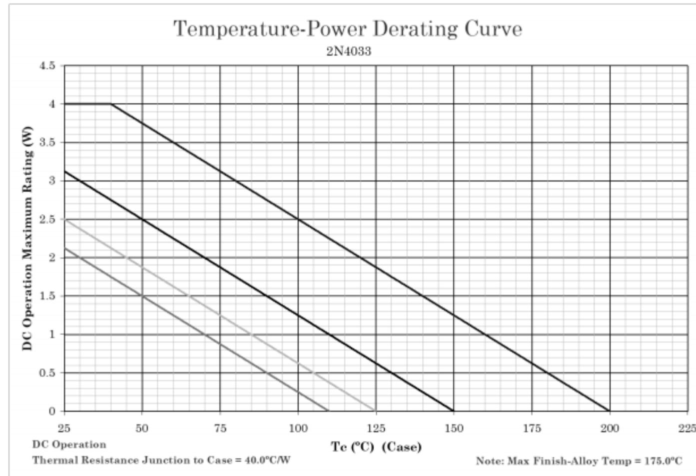
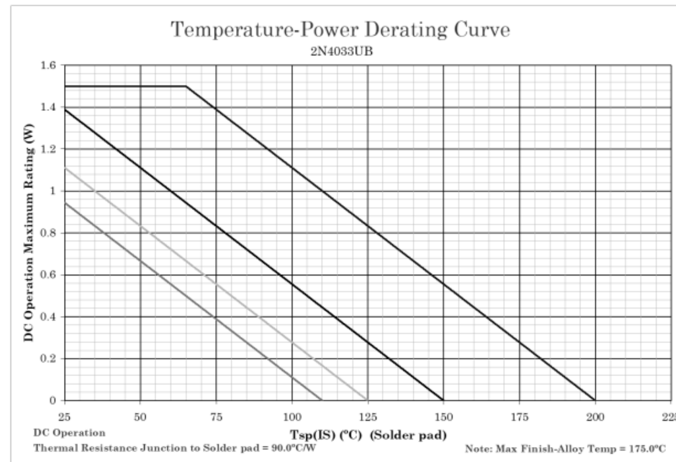
Temperature-Power Derating Curves



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 9. Derating for 2N4033 ($R_{\theta JC}$) (TO-39).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 10. Derating for 2N4033UB ($R_{\theta JSP(IS)}$), infinite sink 3-points.

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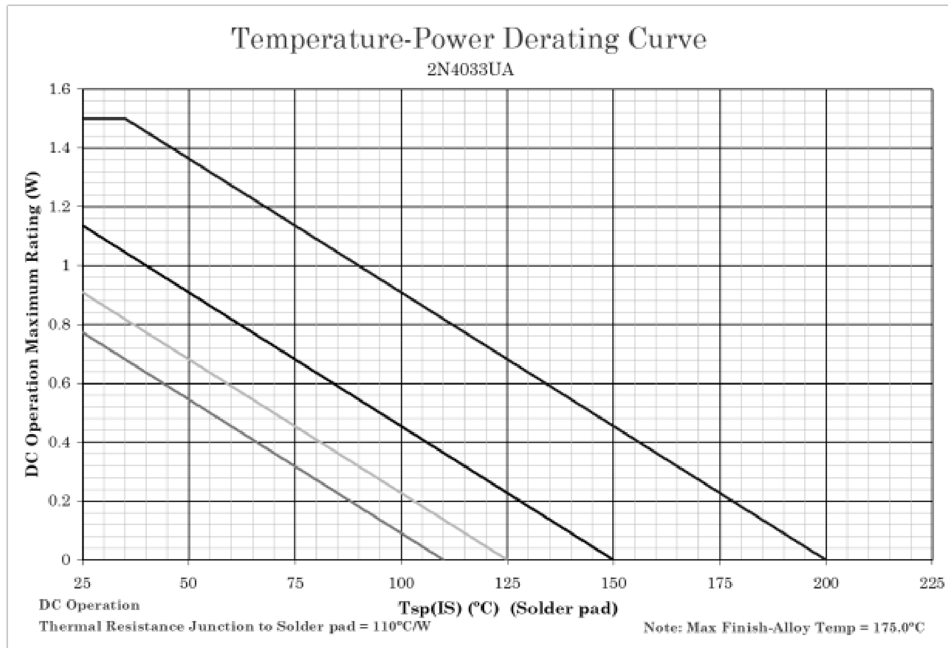
Temperature-Power Derating Curves



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 11. Derating for 2N4033UA ($R_{θJSP(IS)}$).

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Thermal Impedance Curves

Maximum Thermal Impedance

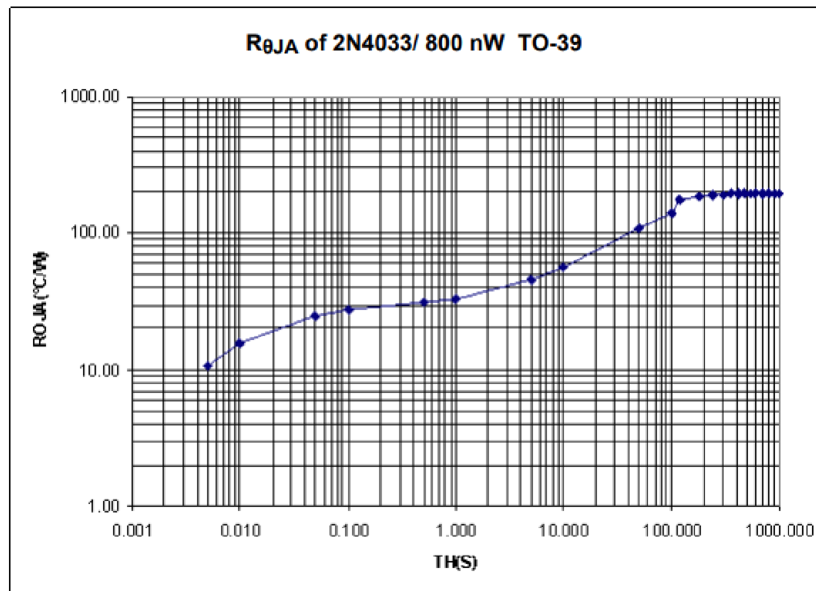

FIGURE 12. Thermal impedance graph ($R_{\theta JA}$) for 2N4033 (TO-39).

Maximum Thermal Impedance

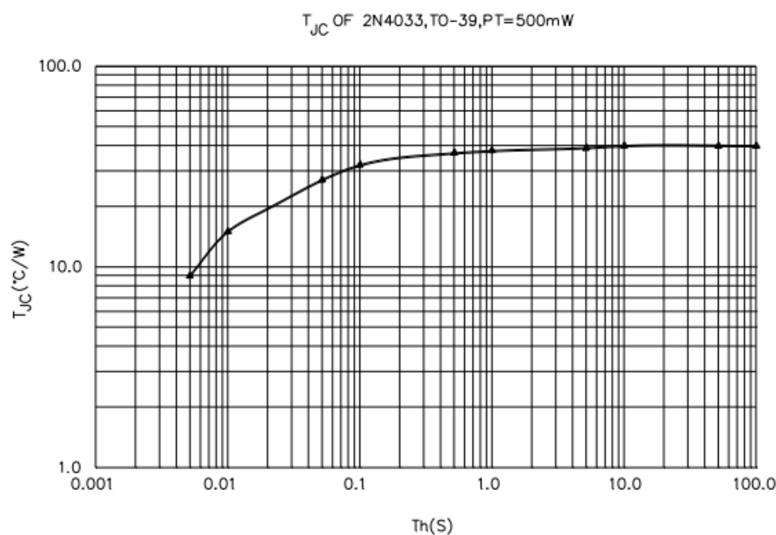

FIGURE 13. Thermal impedance graph ($R_{\theta JC}$) for 2N4033 (TO-39).

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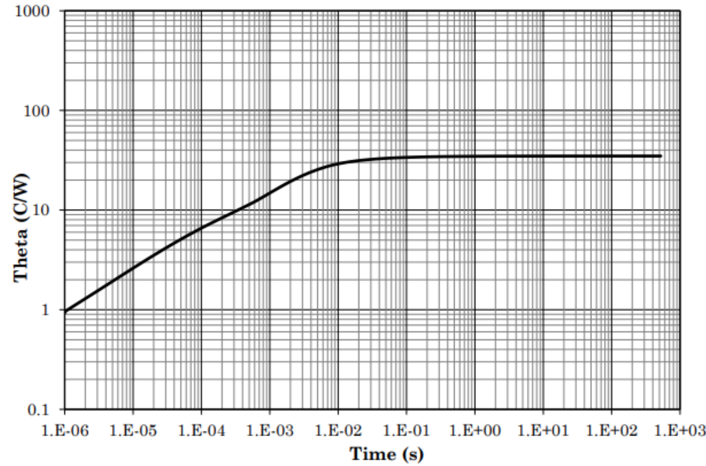
Thermal Impedance Curves

Maximum Thermal Impedance



* FIGURE 13a. Thermal impedance graph ($R_{θJC}$) for Kovar 2N4033 (TO-39).

Maximum Thermal Impedance

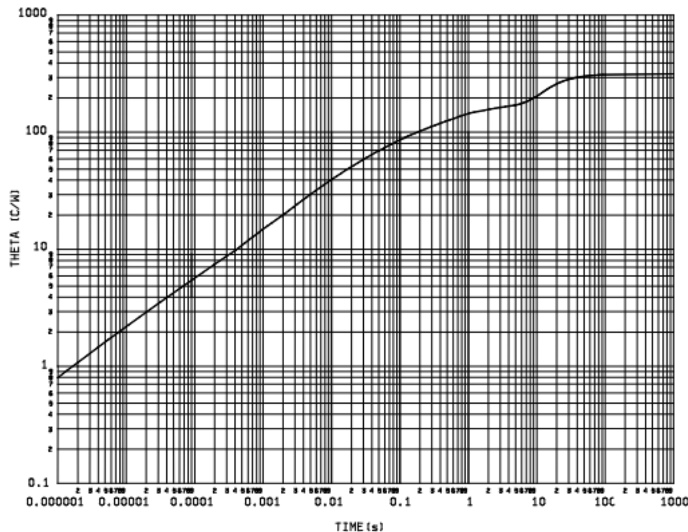


FIGURE 14. Thermal impedance graph ($R_{θJA}$) for 2N4029 (TO-18).

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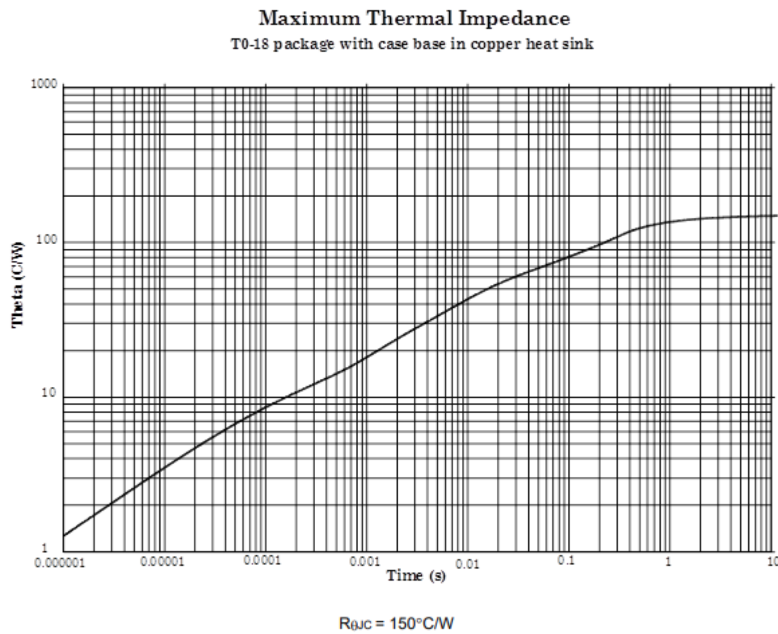
Thermal Impedance Curves



$R_{\theta JC}$ = 150°C/W

FIGURE 15. Thermal impedance graph ($R_{\theta JC}$) for 2N4029 (TO-18).

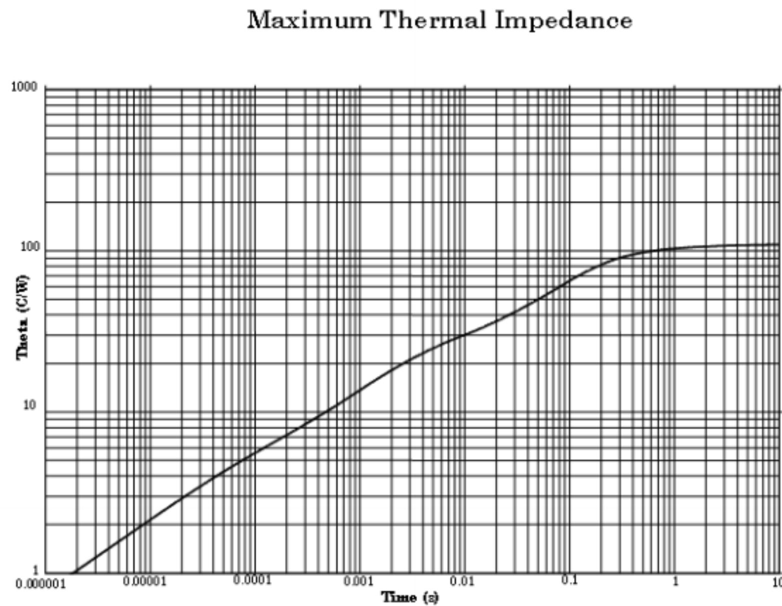


FIGURE 16. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N4033 (UA).

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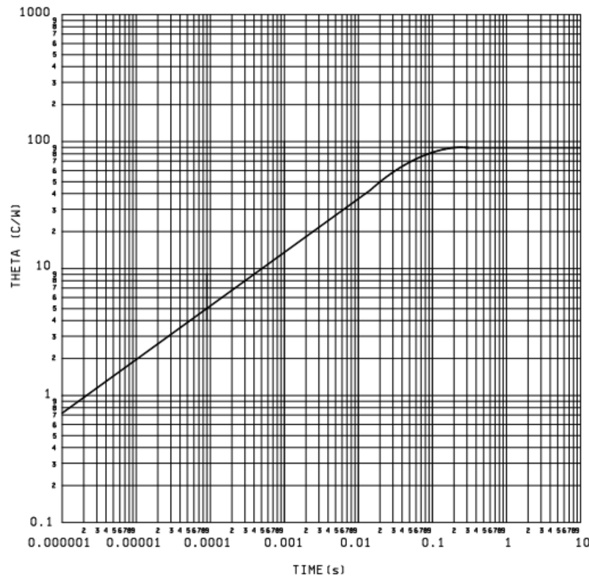
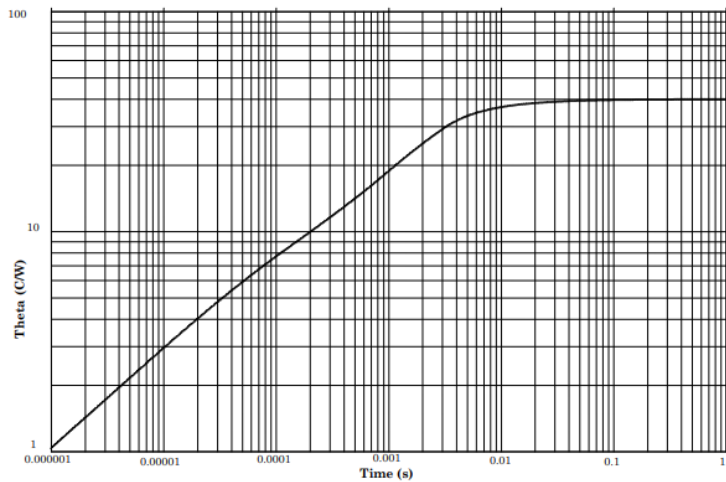
Thermal Impedance Curves



Ceramic UB package soldered to PCB 3 points solder pad (infinite sink to PCB).
$R_{\theta JSP(IS)}$ = 90°C/W

FIGURE 17. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N4029 (UB).



2N4033UA 4 point solder pad (adhesive mount to PCB), $R_{\theta JSP(AM)}$ = 40°C/W

FIGURE 18. Thermal impedance graph $R_{\theta JSP(AM)}$ for 2N4033UA.

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