2N3902 & 2N5157

NPN High Power Silicon Transistors

Rev. V4

Features

- Available in JAN, JANTX, JANTXV per MIL-PRF-19500/371
- TO-3 (TO-204AA) Package
- Designed for Use in High Voltage Inverters, Converters, Switching Regulators and Line Operated Amplifiers

Electrical Characteristics (T_A = +25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Cutoff Current	V_{CE} = 400 V dc, 2N3902 V_{CE} = 500 V dc, 2N5157	I_{CEO}	µA dc	—	100 100
Collector - Emitter Cutoff Current	V_{BE} = 1.5 V dc, V_{CE} = 700 V dc	I_{CEX1}	µA dc	—	20
Collector - Emitter Cutoff Current	V_{BE} = 5 V dc, 2N3902 V_{BE} = 6 V dc, 2N5157	I_{EBO}	µA dc	—	200 200
Forward Current Transfer Ratio	I_C = 0.5 A dc; V_{CE} = 5 V dc I_C = 1.0 A dc; V_{CE} = 5 V dc I_C = 2.5 A dc; V_{CE} = 5 V dc I_C = 3.5 A dc; V_{CE} = 5 V dc	h_{FE}	-	25 30 10 5	90
Collector - Emitter Saturation Voltage	I_C = 1.0 A dc; I_B = 0.1 A dc I_C = 3.5 A dc; I_B = 0.7 A dc	$V_{CE(SAT)1}$ $V_{CE(SAT)2}$	V dc	—	0.8 2.5
Base - Emitter Saturation Voltage	I_C = 1.0 A dc; I_B = 0.1 A dc I_C = 3.5 A dc; I_B = 0.7 A dc	$V_{BE(SAT)1}$ $V_{BE(SAT)2}$	V dc	—	1.5 2.0
Collector - Emitter Sustaining Voltage	I_C = 100mA dc 2N3902 2N5157	$V_{CEO(SUS)}$	V dc	—	325 400
Collector - Emitter Cutoff Current	T_A = +150°C V_{BE} = 1.5 V dc V_{CE} = 400 V dc, 2N3902 V_{CE} = 500 V dc, 2N5157	I_{CEX2}	µA dc	—	300 300
Forward - Current Transfer Ratio	T_A = -55°C V_{CE} = 5.0 V dc; I_C = 1.0 A dc	h_{FE5}		10	—
Small-Signal Short-Circuit Forward Current Transfer Ratio	I_C = 0.2 A dc; V_{CE} = 10 Vdc; f = 1 MHz	$\lvert h_{fe} \rvert$	-	2.5	25
Output Capacitance	V_{CB} = 10 Vdc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}	pF	—	250

(Continued next page)

For further information and support please visit:
info@vptcomponents.com

Electrical Characteristics (T_A = +25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Switching Characteristics					
Turn-On Time	V_{CC} = 125 Vdc; I_C = 1.0 A dc; I_{B1} = 0.1 A dc	t_{on}	µs	—	0.8
Turn-Off Time	V_{CC} = 125 V dc; I_C = 1.0 A dc; I_{B1} = 0.1 A dc; $-I_{B2}$ = 0.50 A dc	t_{off}	µs	—	1.7
Safe Operating Area					

DC Tests: T_C = +25°C, I Cycle, t = 1.0 s (see Fig. 3 of MIL-PRF-19500/371)
Test 1: V_{CE} = 28.6 Vdc, I_C = 3.5 A dc
Test 2: V_{CE} = 70 Vdc, I_C = 1.43 A dc
Test 3: V_{CE} = 325 Vdc, I_C = 55 mA dc, 2N3902
V_{CE} = 400 Vdc, I_C = 35 mA dc, 2N5157

Switching Tests:
Load Condition C (unclamped inductive load): T_C = +25°C, duty cycle <10%; R_S = 0.1 Ω (See Fig. 4 of MIL-PRF-19500/371)
Test 1: t_p = approximately 3 ms (vary to obtain I_C), R_{BB1} = 20 Ω, V_{BB1} = 10 Vdc; R_{BB2} = 3 kΩ,
V_{BB2} = 1.5 V dc, V_{CC} = 50 Vdc, I_C = 3.5 A dc, L = 60 mH, R = 3 Ω; R_L <14 Ω
Test 2: t_p = approximately 3 ms (vary to obtain I_C), R_{BB1} = 100 Ω, V_{BB1} = 10 Vdc; R_{BB2} = 3 kΩ,
V_{BB2} = 1.5 V dc, I_C = 0.6 A dc, V_{CC} = 50 Vdc, L = 200 mH, R = 8 Ω; R_L <83 Ω

Load Condition (clamped inductive load): T_C = +25°C, duty cycle <10% (See Fig. 5 of MIL-PRF-19500/371)
Test 1: t_p = approximately 30 ms (vary to obtain I_C), R_S = 0.1 Ω, R_{BB1} = 20 Ω, V_{BB1} = 10 Vdc;
R_{BB2} = 100 Ω, V_{BB2} = 1.5 Vdc, V_{CC} = 50 Vdc, I_C = 3.5 Adc, L = 60 mH, R = 3 Ω; R_L <0 Ω
(A suitable clamping circuit or diode can be used.)
Clamp Voltage = 400 +0, -5 Vdc 2N3902
Clamp Voltage = 500 +0, -5 Vdc 2N5157
(Clamped voltage must be reached)

Absolute Maximum Ratings (T_A = +25°C unless otherwise noted)

Ratings	Symbol	Value
Collector - Emitter Voltage 2N3902 2N5157	V_{CEO}	400 V dc 500 V dc
Emitter - Base Voltage 2N3902 2N5157	V_{EBO}	5 V dc 6 V dc
Collector - Base Voltage	V_{CBO}	700 V dc
Base Current	I_B	2.0 A dc
Collector Current	I_C	3.5 A dc
Total Power Dissipation	P_T	5 W
Total Power Dissipation T_C = +25°C	P_T (1)	125 W
Operating & Storage Temperature Range	T_J, T_{STG}	-65°C to +200°C

Thermal Characteristics

Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.25°C/W

(1) See figures 4, 5 and 6 of MIL-PRF-19500/371 for temperature-power derating curves.
(2) For thermal impedance curves, see figures 7, 8 and 9 of MIL-PRF-19500/371.

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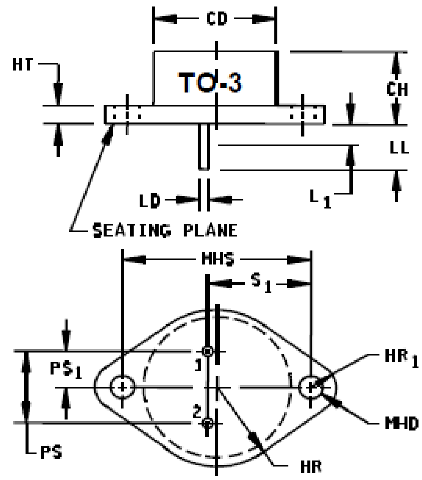
Outline Drawing (TO-3)

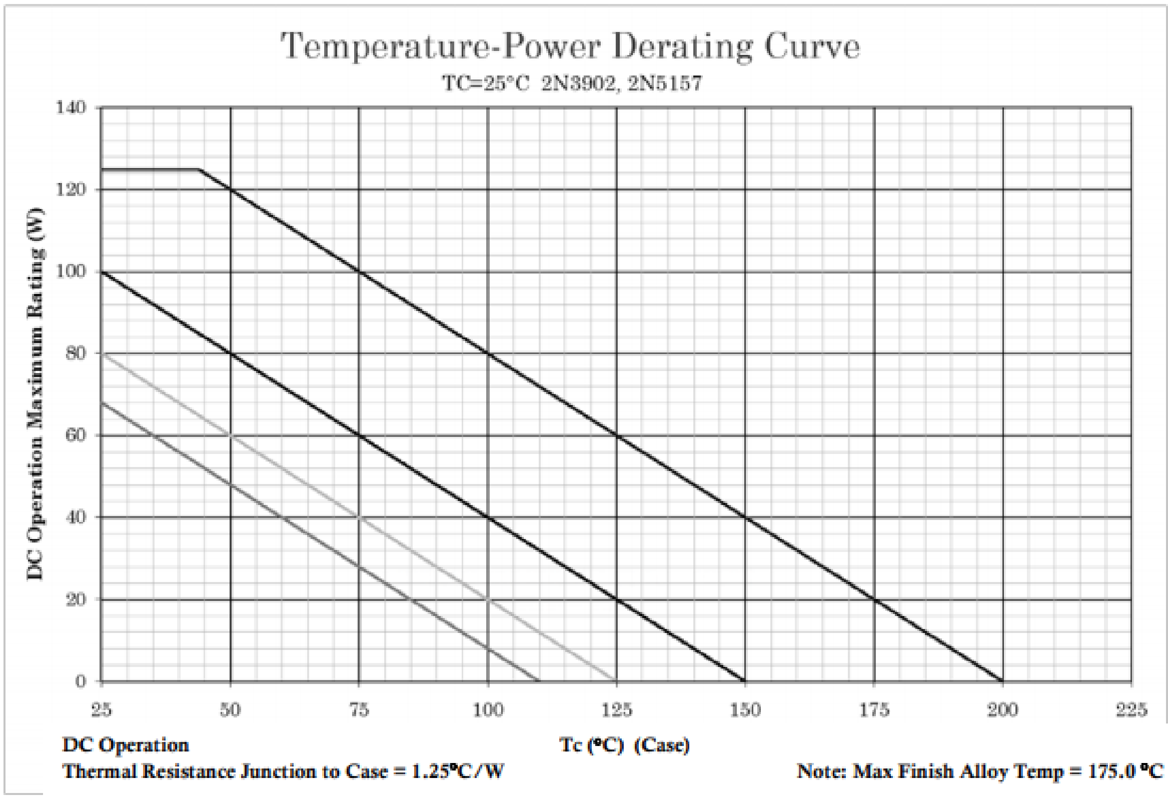


Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.22	3
CH	.250	.328	6.35	8.33	
HR	.495	.525	12.57	13.34	
HR_1	.131	.188	3.33	4.78	6
HT	.060	.135	1.52	3.43	
LD	.038	.043	0.97	1.09	4, 5, 9
LL	.312	.500	7.92	12.70	4, 5, 9
L_1		.050		1.27	5, 9
MHD	.151	.161	3.84	4.09	7
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	
PS_1	.205	.225	5.21	5.72	5
S_1	.655	.675	16.64	17.15	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Body contour is optional within zone defined by CD.
4. These dimensions shall be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement shall be made at seating plane.
5. Both terminals.
6. At both ends.
7. Two holes.
8. Terminal 1 is the emitter, terminal 2 is base. The collector shall be electrically connected to the case.
9. LD applies between L_1 and LL. Lead diameter shall not exceed twice LD within L_1.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
11. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.

* FIGURE 1. Physical dimensions, 2N3902, 2N5157 (modified TO-204AA, similar to TO-3).

Temperature-Power Derating Curve

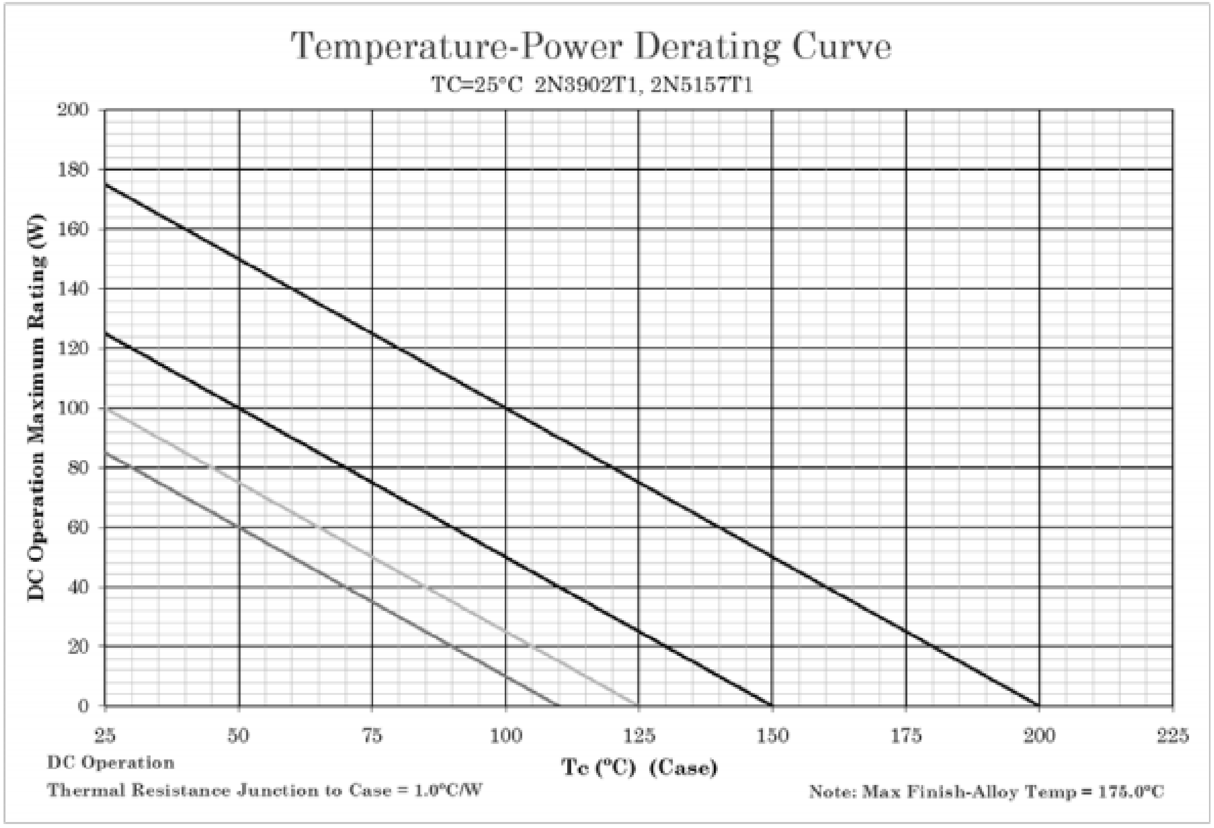


NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and $+110°C$ to show power rating where most users want to limit T_J in their application.

FIGURE 4. Temperature-power derating graph (TO-3), 2N3902 and 2N5157.

Temperature-Power Derating Curve



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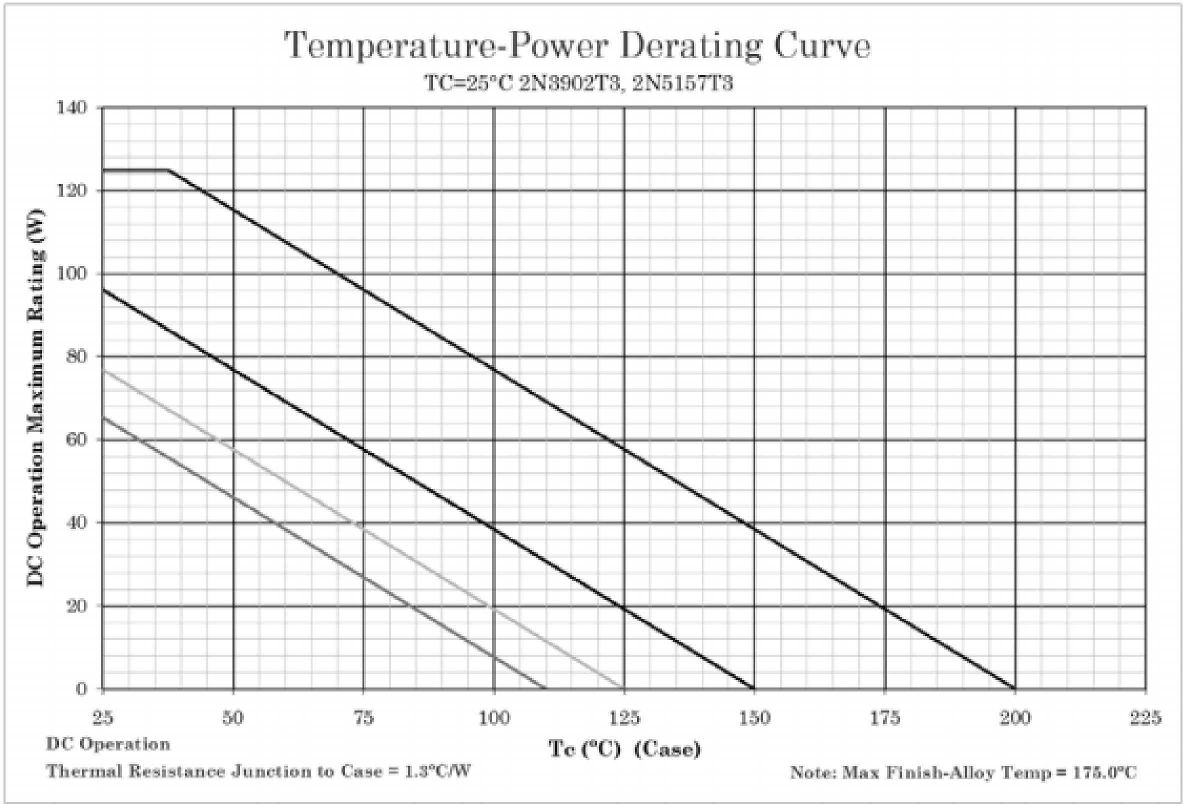
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 5. Temperature-power derating graph (TO-254), 2N3902T1 and 2N5157T1.

Temperature-Power Derating Curve

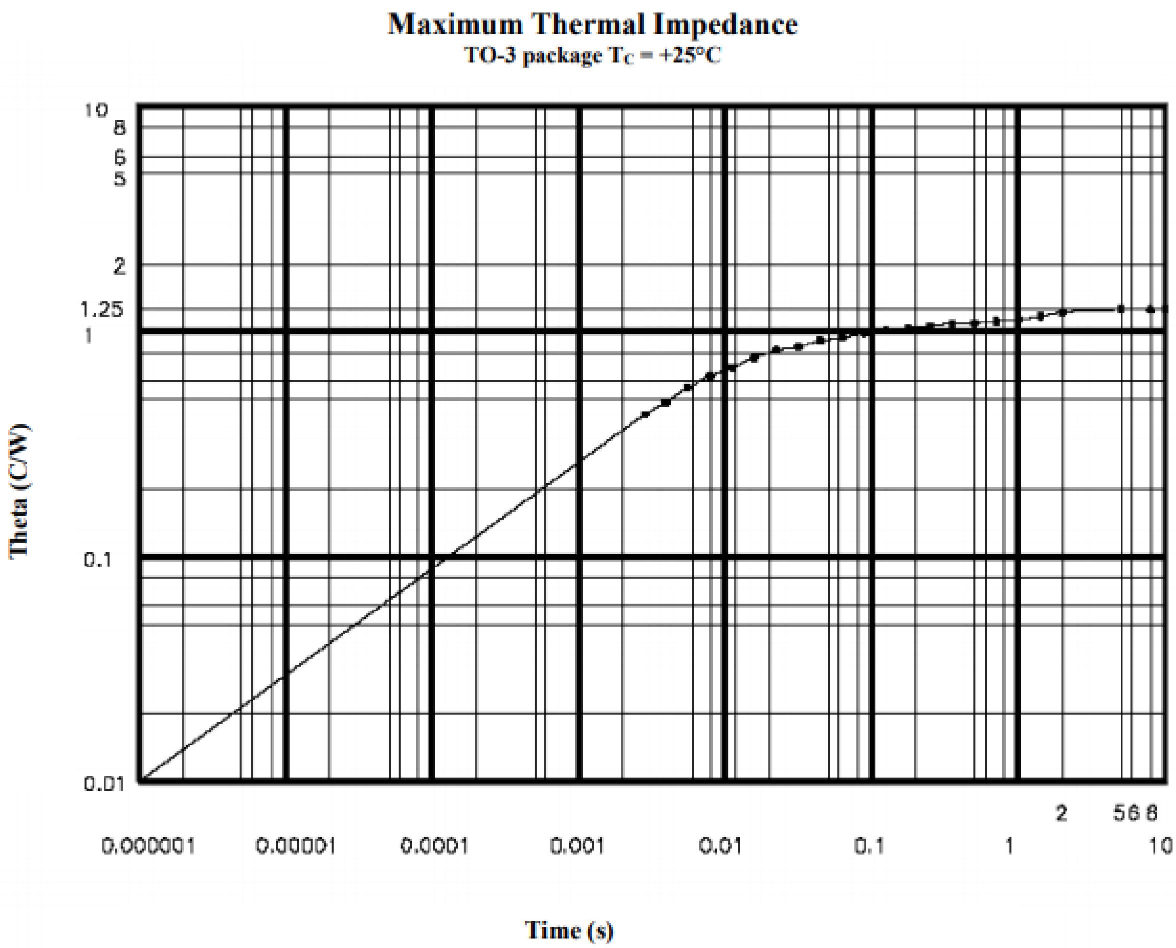


NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 6. Temperature-power derating graph (TO-257), 2N3902T3 and 2N5157T3.

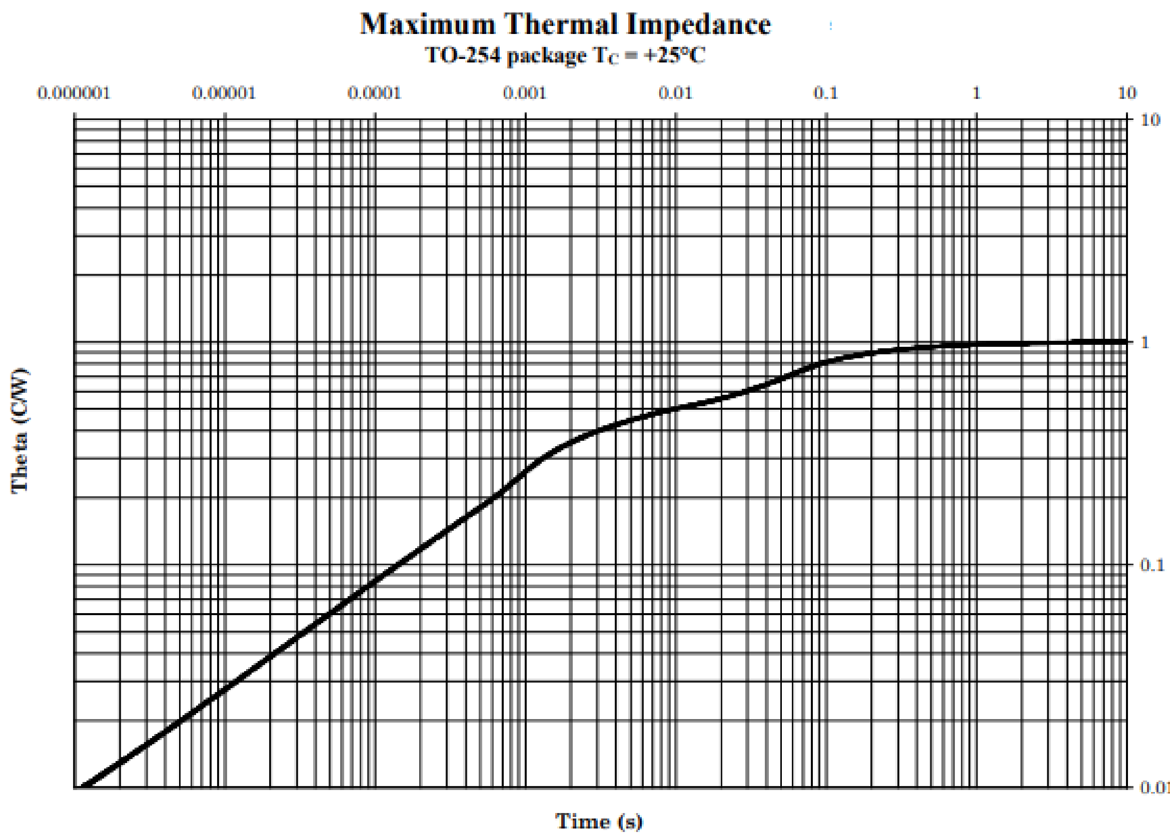
Thermal Impedance Curve



$R_{\theta JC}$ = 1.25°C/W max.

FIGURE 7. Thermal impedance graph (2N3902 and 2N5157).

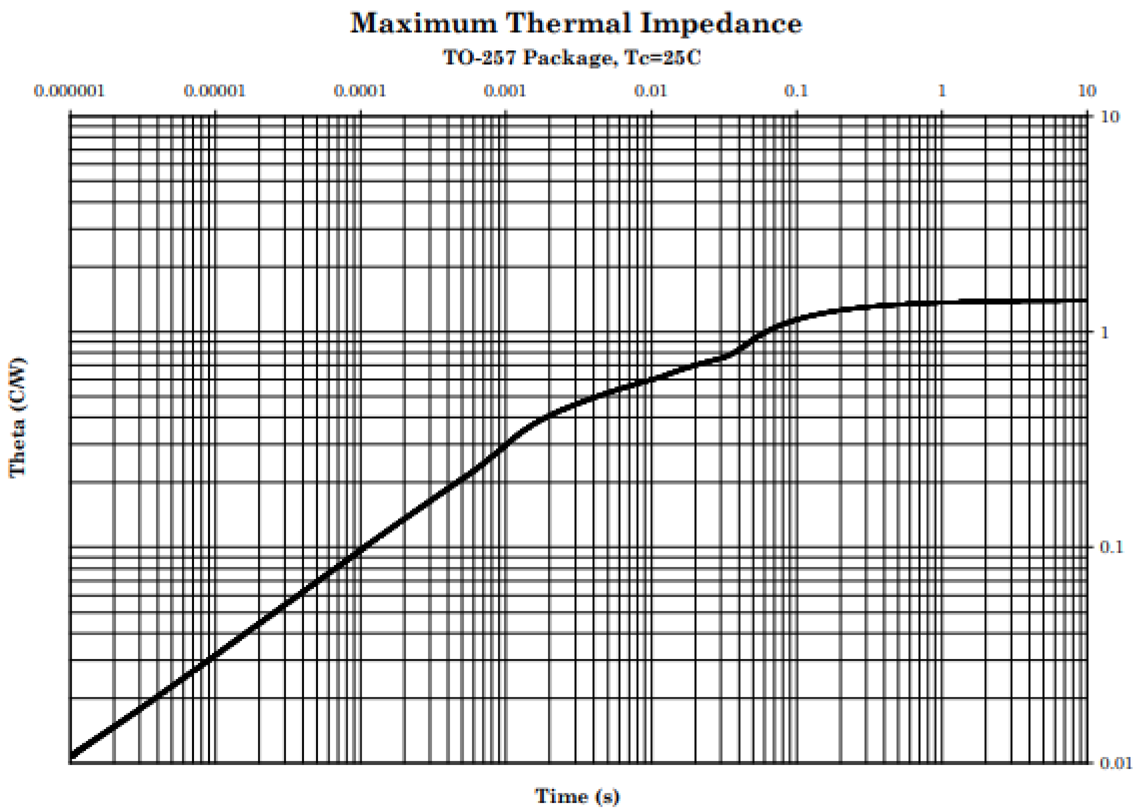
Thermal Impedance Curve



$R_{\theta JC}$ = 1.0°C/W max.

FIGURE 8. Thermal impedance graph (2N3902T1 and 2N5157T1).

Thermal Impedance Curve



$R_{\theta JC}$ = 1.3°C/W max.

FIGURE 9. Thermal impedance graph (2N3902T3, and 2N5157T3).