

# 2N3439, 2N3440

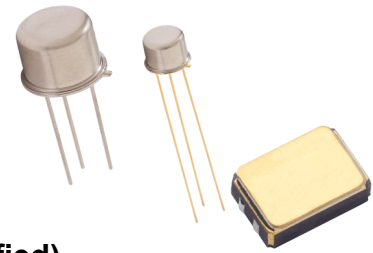


## NPN Low Power, High Voltage Silicon Transistor

Rev. V1

### Features

- Available in JAN, JANTX and JANTXV per MIL-PRF-19500/368
- TO-39, TO-5, and UA Package Types
- Suitable For Drivers in High-Voltage Low Current Inverters, Switching and Series Regulators



### Electrical Characteristics ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Emitter - Base Cutoff Current	$V_{EB} = 7.0 \text{ V dc}$	$I_{EBO1}$	$\mu\text{A dc}$	—	10
Collector - Emitter Cutoff	$V_{CE} = 300 \text{ V dc}$ 2N3439, L, UA $V_{CE} = 200 \text{ V dc}$ 2N3440, L, UA	$I_{CEO}$	$\mu\text{A dc}$		2 2
Collector - Emitter Cutoff Current	$V_{BE} = -1.5 \text{ V dc}$ $V_{CE} = 450 \text{ V dc}$ 2N3439, L, UA $V_{CE} = 300 \text{ V dc}$ 2N3440, L, UA	$I_{CEX}$	$\mu\text{A dc}$	—	5 5
Collector - Base Cutoff Current	$V_{CB} = 360 \text{ V dc}$ 2N3439, L, UA $V_{CB} = 250 \text{ V dc}$ 2N3440, L, UA	$I_{CBO1}$	$\mu\text{A dc}$	—	2 2
Collector - Base Cutoff Current	$V_{CB} = 450 \text{ V dc}$ 2N3439, L, UA $V_{CB} = 300 \text{ V dc}$ 2N3440, L, UA	$I_{CBO2}$	$\mu\text{A dc}$	—	5 5
Base - Emitter Voltage (saturated)	$I_C = 50 \text{ mA dc}$ , $I_B = 4 \text{ mA dc}$	$V_{BE(sat)}$	V dc		1.3
Collector - Emitter Voltage (saturated)	$I_C = 50 \text{ mA dc}$ , $I_B = 4 \text{ mA dc}$	$V_{CE(sat)}$	V dc		0.5
Forward Current Transfer Ratio	$V_{CE} = 10 \text{ Vdc}$ , $I_C = 20 \text{ mA dc}$ $V_{CE} = 10 \text{ Vdc}$ , $I_C = 2 \text{ mA dc}$ $V_{CE} = 10 \text{ Vdc}$ , $I_C = 0.2 \text{ mA dc}$	$h_{FE}$	-	40 30 10	160
Collector - Emitter Cutoff Current	$T_A = +150^\circ\text{C}$ $V_{CB} = 360 \text{ V dc}$ 2N3439, L, UA $V_{CB} = 250 \text{ V dc}$ 2N3440, L, UA	$I_{CBO3}$	$\mu\text{A dc}$		6 6
Forward - Current Transfer Ratio	$T_A = -55^\circ\text{C}$ $V_{CE} = 10 \text{ V dc}$ , $I_C = 20 \text{ mA dc}$	$h_{FE4}$		15	

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Rev. V1

### Electrical Characteristics

Parameter	Test Conditions	Symbol	Units	Min.	Max.
<b>Dynamic Characteristics</b>					
Magnitude of Common-Emitter Small Signal Short Circuit Forward-Current Transfer Ratio	$V_{CE} = 10 \text{ V dc}, I_C = 10 \text{ mA dc}, f = 5 \text{ MHz}$	$ h_{FE} $		3	15
Output Capacitance (Input Open Circuited)	$V_{CB} = 10 \text{ V dc}, I_E = 0, 100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	$C_{obo}$	pF	—	10
Small-Signal Short-Circuit Forward-Current Transfer Ratio	$V_{CE} = 10 \text{ V dc}, I_C = 5 \text{ mA dc}, f = 1 \text{ kHz}$	$h_{fe}$		25	—
Input Capacitance (Output Open Circuited)	$V_{CB} = 5 \text{ V dc}, I_E = 0, 100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	$C_{ibo}$	pF	—	75
<b>Switching Characteristics</b>					
Turn-On Time	$V_{CC} = 200 \text{ V dc}, I_C = 20 \text{ mA dc}, I_{B1} = 2 \text{ mA dc}$	$t_{on}$	$\mu\text{s}$	—	1.0
Turn-Off Time	$V_{CC} = 200 \text{ V dc}, I_C = 20 \text{ mA dc}, I_{B1} = -I_{B2} = 2 \text{ mA dc}$	$t_{off}$	$\mu\text{s}$	—	10

### Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Ratings	Symbol	2N3439	2N3440
Collector - Emitter Voltage	$V_{CEO}$	350 V dc	250 V dc
Collector - Base Voltage	$V_{CBO}$	450 V dc	300 V dc
Emitter - Base Voltage	$V_{EBO}$	7.0 V dc	
Collector Current	$I_C$	1.0 A dc	
Junction & Storage Temperature Range	$T_J, T_{STG}$	-65°C to +200°C	

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### Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Thermal Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Ambient 2N3439, 2N3439L 2N3439UA 2N3440, 2N3440L 2N3440UA	$R_{\theta JA}^{(3)}$	175°C/W
Thermal Resistance, Junction to Case 2N3439, 2N3440 2N3439L, 2N3440L 2N3439UA, 2N3440UA	$R_{\theta JC}^{(3)}$	30°C/W N/A
Thermal Resistance, Junction to Solder Pad 2N3439UA, 2N3440UA	$R_{\theta JSP}^{(3)}$	70°C/W

(1) For thermal impedance curves see figures 10, 11, 12, and 13 of MIL-PRF-19500/368

# 2N3439, 2N3440



## NPN Low Power, High Voltage Silicon Transistor

Rev. V1

### Absolute Maximum Ratings ( $T_A = +25^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Max. Value
$T_A = +25^{\circ}\text{C}$ 2N3439, 2N3439L 2N3439UA, 2N3439U4 2N3440, 2N3440L 2N3440UA, 2N3440U4	$P_T^{(1)}$	0.8 W
$T_C = +25^{\circ}\text{C}$ 2N3439, 2N3440 2N3439L, 2N3440L 2N3439UA, 2N3440UA 2N3439U4, 2N3440U4	$P_T^{(2)}$	5.0 W N/A 5 W
$T_{SP} = +25^{\circ}\text{C}$ 2N3439UA, 2N3440UA	$P_T^{(2)}$	2.0 W

- (1) For derating see figures 6 of MIL-PRF-19500/368  
 (2) For derating see figures 7, 8, and 9 of MIL-PRF-19500/368

### Safe Operating Area

DC Tests:	$T_C = +25^{\circ}\text{C}$ ; 1 Cycle; $t = 1.0\text{s}$	
Test 1:	$V_{CE} = 5\text{ V dc}$ ; $I_C = 1.0\text{ A dc}$ All types	
Test 2:	$V_{CE} = 350\text{ V dc}$ ; $I_C = 14\text{ mA dc}$	2N3439, 2N3439L, 2N3439UA
Test 3:	$V_{CE} = 250\text{ V dc}$ ; $I_C = 20\text{ mA dc}$	2N3440, 2N3440L, 2N3440UA

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Breakdown Voltage, Collector-Emitter	$I_C = 10\text{ mA}$ , $R_{BB1} = 470\ \Omega$ , $V_{BB1} = 6\text{V}$ , $f = 30\text{ to }60\text{ Hz}$ 2N3439, L, UA 2N3440, L, UA	$V_{BR(CEO)}$	V dc	350 250	—

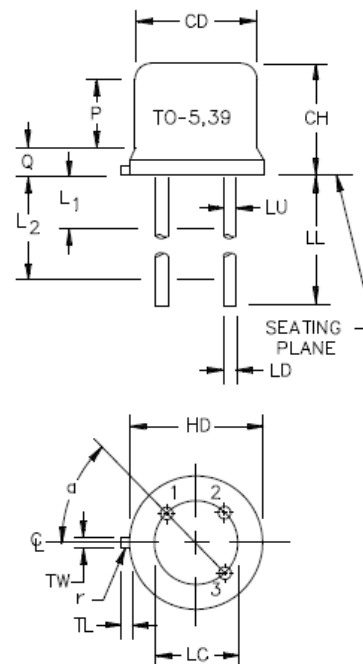
# 2N3439, 2N3440

## NPN Low Power, High Voltage Silicon Transistor

Rev. V1

### Outline Drawing (TO-5, TO-39)

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	6
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		7
LD	.016	.019	0.41	0.48	8,9
LL	See note 14				
LU	.016	.019	0.41	0.48	8,9
L <sub>1</sub>		.050		1.27	8,9
L <sub>2</sub>	.250		6.35		8,9
P	.100		2.54		7
Q		.030		0.76	5
TL	.029	.045	0.74	1.14	3,4
TW	.028	.034	0.71	0.86	3
r		.010		0.25	10
α	45° TP		45° TP		7



#### NOTES:

- Dimensions are in inches.
- Millimeters are given for general information only.
- Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
- Dimension TL measured from maximum HD.
- Body contour optional within zone defined by HD, CD, and Q.
- CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
- Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by gauging procedure.
- Dimension LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between L<sub>2</sub> and LL minimum. Diameter is uncontrolled in and beyond LL minimum.
- All three leads.
- The collector shall be internally connected to the case.
- Dimension r (radius) applies to both inside corners of tab.
- In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi$ x symbology.
- Lead 1 = emitter, lead 2 = base, lead 3 = collector.
- For transistor types 2N3439L and 2N3440L (TO-5), dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max. For transistor types 2N3439 and 2N3440 (TO-39), dimension LL = .5 inch (12.70 mm) min. and .750 inch (19.05 mm) max.

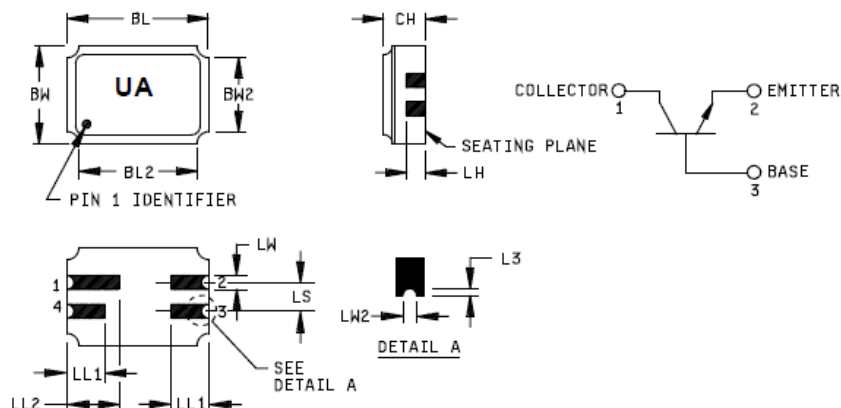
FIGURE 1. Physical dimensions (similar to TO-5 and TO-39).

# 2N3439, 2N3440

## NPN Low Power, High Voltage Silicon Transistor

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### Outline Drawing (UA Package)



Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.90	3
L3	.003		0.08		5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

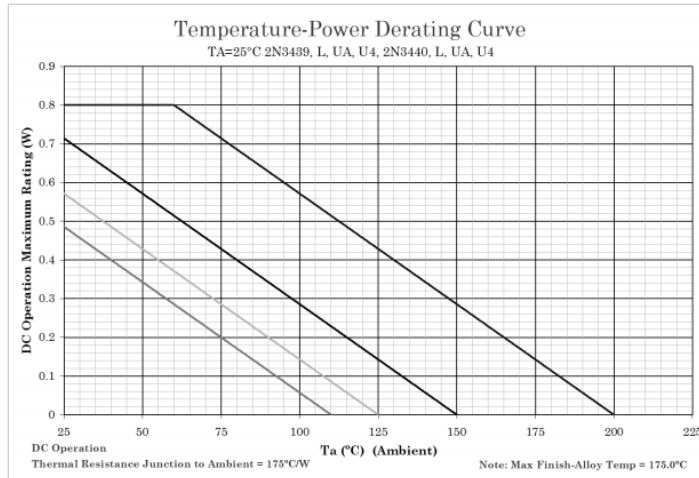
Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

#### NOTES:

- Dimensions are in inches.
- Millimeters are given for general information only.
- Dimension "CH" controls the overall package thickness. When a window lid is used, dimension "CH" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
- The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
- Dimensions "LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW2" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
- The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
- In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.

FIGURE 3. Physical dimensions, surface mount (2N3439UA, 2N3440UA) version.

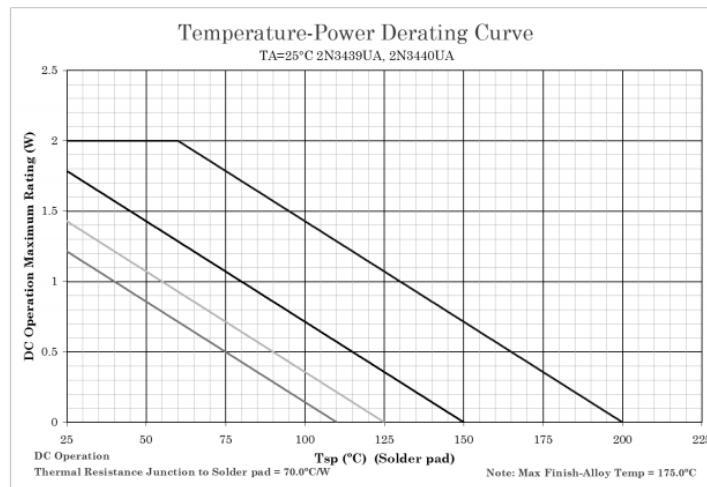
### Temperature-Power Derating Curve



NOTES:

1. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 6. Temperature-power derating for all types R<sub>0JA</sub> (TO-5, TO-39, UA, and U4).

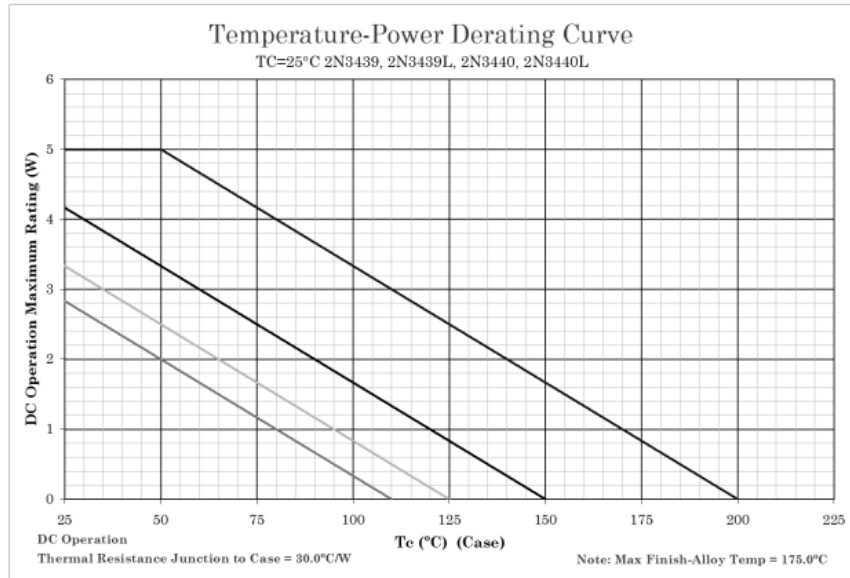


NOTES:

1. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
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3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 7. Temperature-power derating for 2N3439UA and 2N3440UA.

### Temperature-Power Derating Curve



#### NOTES:

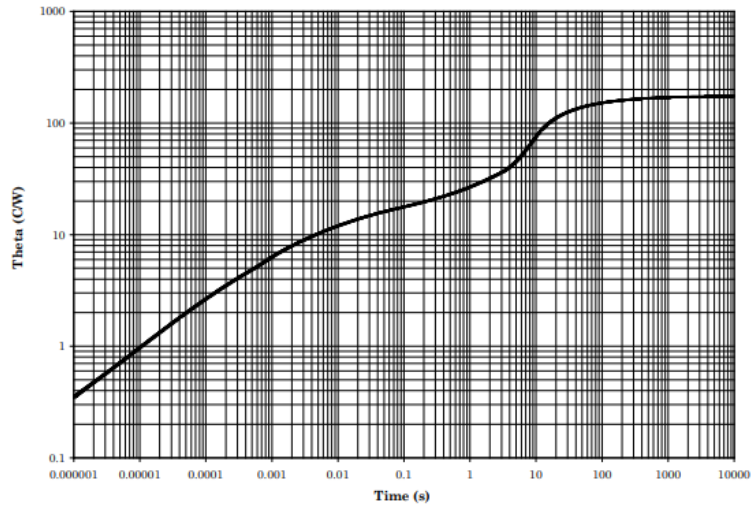
1. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 9. Temperature-power derating for 2N3439, 2N3439L, 2N3440, and 2N3440L.



### Thermal Impedance Curves

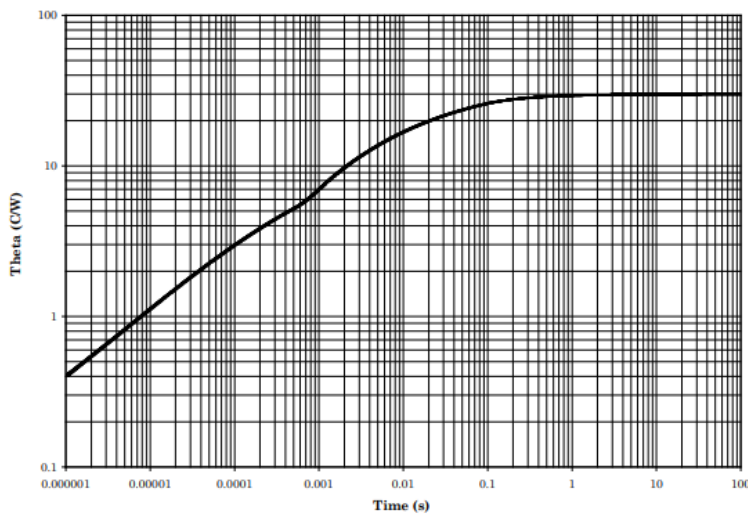
Maximum Thermal Impedance



$T_A = +25^{\circ}\text{C}$ ,  $P_T = 0.8\text{W}$ , thermal resistance  $R_{\theta JA} = 175^{\circ}\text{C/W}$ .

FIGURE 10. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N3439, 2N3439L, 2N3440, and 2N3440L (TO-5, TO-39, U4, and UA).

Maximum Thermal Impedance

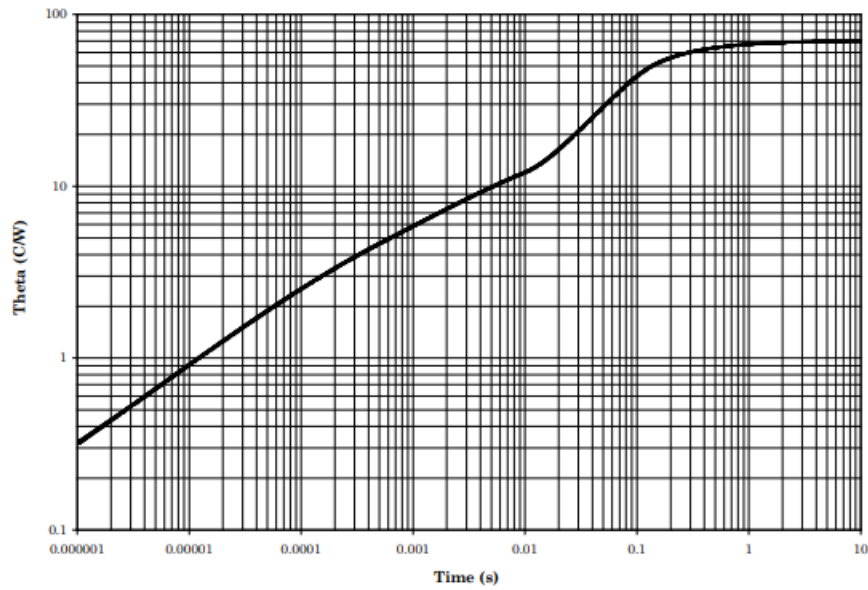


$T_C = +25^{\circ}\text{C}$ ,  $P_T = 5.0\text{W}$ , thermal resistance  $R_{\theta JC} = 30^{\circ}\text{C/W}$ , steel.

FIGURE 11. Thermal impedance graph ( $R_{\theta JC}$ ) for 2N3439, 2N3439L, 2N3440, and 2N3440L (TO-5 and TO-39).

### Thermal Impedance Curves

Maximum Thermal Impedance



$T_c = +25^\circ\text{C}$ , thermal resistance  $R_{\theta\text{JSP}} = 70^\circ\text{C/W}$ ,  $P_{\text{diss}} = 2\text{W}$ .

FIGURE 12. Thermal impedance graph ( $R_{\theta\text{JSP}}$ ) for 2N3439UA and 2N3440UA.

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