# 2N6051 & 2N6052

## PNP Darlington Power Silicon Transistors

Rev. V3

### Features

- Available in JAN, JANTX, JANTXV per MIL-PRF-19500/501
- TO-3 (TO-204AA) Package
- Ideal for High Gain Amplifier and Switching Applications

### Electrical Characteristics ($T_A$ = +25$^o$C unless otherwise noted)

| Parameter | Test Conditions | Symbol | Units | Min. | Max. |
|---|---|---|---|---|---|
| | | | | | |
| Collector - Emitter Breakdown Voltage | $I_C$ = -10 mA dc, 2N6051<br>$I_C$ = -10 mA dc, 2N6052 | $V_{(BR)CEO}$ | V dc | -80<br>-100 | — |
| Collector - Emitter Cutoff Current | $V_{CE}$ = -40 V dc, 2N6051<br>$V_{CE}$ = -50 V dc, 2N6052 | $I_{CEO}$ | mA dc | — | -1 |
| Collector - Emitter Cutoff Current | $V_{CE}$ = -80 V dc, $V_{BE}$ = +1.5 V dc, 2N6051<br>$V_{CE}$ = -100 V dc, $V_{BE}$ = +1.5 V dc, 2N6052 | $I_{CEX1}$ | mA dc | — | -.01 |
| Emitter - Base Cutoff Current | $V_{EB}$ = -5 Vdc | $I_{EBO}$ | mA dc | — | -2 |
| | | | | | |
| Forward Current Transfer Ratio | $V_{CE}$ = -3 V dc, $I_C$ = -1 A dc<br>$V_{CE}$ = -3 V dc, $I_C$ = -6 A dc<br>$V_{CE}$ = -3 V dc, $I_C$ = -12 A dc | $h_{FE}$ | - | 1,000<br>1,000<br>150 | 18,000 |
| Collector - Emitter Saturation Voltage | $I_C$ = -12 A dc, $I_B$ = -120 mA dc<br>$I_C$ = -6 A dc, $I_B$ = -24 mA dc | $V_{CE(sat)1}$<br>$V_{CE(sat)2}$ | V dc | — | -3.0<br>-2.0 |
| Base - Emitter Saturation Voltage | $I_C$ = -12 A dc, $I_B$ = -120 mA dc | $V_{BE(sat)}$ | V dc | — | -4.0 |
| Base - Emitter Voltage (non-saturated) | $I_C$ = -6 A dc, $V_{CE}$ = -3 V dc | $V_{BE}$ | V dc | — | -2.8 |
| Collector - Emitter Cutoff Current | $T_A$ = +150$^o$C<br>$V_{CE}$ = -80 V dc, $V_{BE}$ = +1.5 V dc, 2N6051<br>$V_{CE}$ = -100 V dc, $V_{BE}$ = +1.5 V dc, 2N6052 | $I_{CEX2}$ | mA dc | — | -5.0<br>-5.0 |
| Forward Current Transfer Ratio | $T_A$ = -55$^o$C<br>$V_{CE}$ = -3 V dc, $I_C$ = -6 A dc | $h_{FE4}$ | - | 300 | |
| **Dynamic Characteristics** | | | | | |
| Magnitude of Small-Signal Short-Circuit Forward - Current Transfer Ratio | $V_{CE}$ = -3 V dc; $I_C$ = -5 A dc; f = 1.0 MHz | $\lvert h_{fe} \rvert$ | - | 10 | 250 |
| Small-Signal Short-Circuit Forward Current Transfer Ratio | $V_{CE}$ = -3 V dc; $I_C$ = -5 A dc; f = 1 kHz | $h_{fe}$ | - | 1000 | |
| Output Capacitance | $V_{CB}$ = -10 V dc; $I_E$ = 0; 100 kHz ≤ f ≤ 1 MHz | $C_{obo}$ | pF | — | 300 |
| **Switching Characteristics** | | | | | |
| Turn-On Time | $V_{CC}$ = -30 V dc; $I_C$ = -5 A dc; $I_{B1}$ = -20 mA dc | $t_{on}$ | µs | — | 2.0 |
| Turn-Off Time | $V_{CC}$ = -30 V dc; $I_C$ = -5 A dc; $I_{B1}$ = $I_{B2}$ = -20 mA dc | $t_{off}$ | µs | — | 10 |





*For further information and support please visit:*
***info@vptcomponents.com***

# 2N6051 & 2N6052

## PNP Darlington Power Silicon Transistors

Rev. V3

### Absolute Maximum Ratings ($T_C$ = +25°C unless otherwise noted)

| Ratings | Symbol | Value |
|---|---|---|
| Collector - Emitter Voltage<br>2N6051<br>2N6052 | $V_{CEO}$ | -80 V dc<br>-100 V dc |
| Collector - Base Voltage<br>2N6051<br>2N6052 | $V_{CBO}$ | -80 V dc<br>-100 V dc |
| Emitter - Base Voltage | $V_{EBO}$ | -5 V dc |
| Collector Current | $I_C$ | -12 A dc |
| Base Current | $I_B$ | -0.2 A dc |
| Total Power Dissipation (1)<br>@ $T_C$ = +25°C<br>@ $T_C$ = +100°C | $P_T$ | 150 W<br>75 W |
| Operating & Storage Temperature Range | $T_J$, $T_{STG}$ | -55°C to +175°C |

(1) Derate linearly @ 1.00 W/°C for $T_C$ >+25°C. (See figure 2 of MIL-PRF-19500/501).

### Thermal Characteristics

| Characteristics | Symbol | Max. Value |
|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 1.0°C/W |

| Safe Operating Area | |
|---|---|
| DC Tests: | $T_C$ = +25°C, +10°C, -0°C, I Cycle, t ≥ 1s; 1 cycle |
| Test 1: | $V_{CE}$ = -12.5 V dc, $I_C$ = -12 A dc |
| Test 2: | $V_{CE}$ = -30 V dc, $I_C$ = -5 A dc |
| Test 3: | $V_{CE}$ = -70 V dc, $I_C$ = -200 mA dc, 2N6051<br>$V_{CE}$ = -90 V dc, $I_C$ = -155 mA dc, 2N6052 |

## Outline Drawing (TO-3)

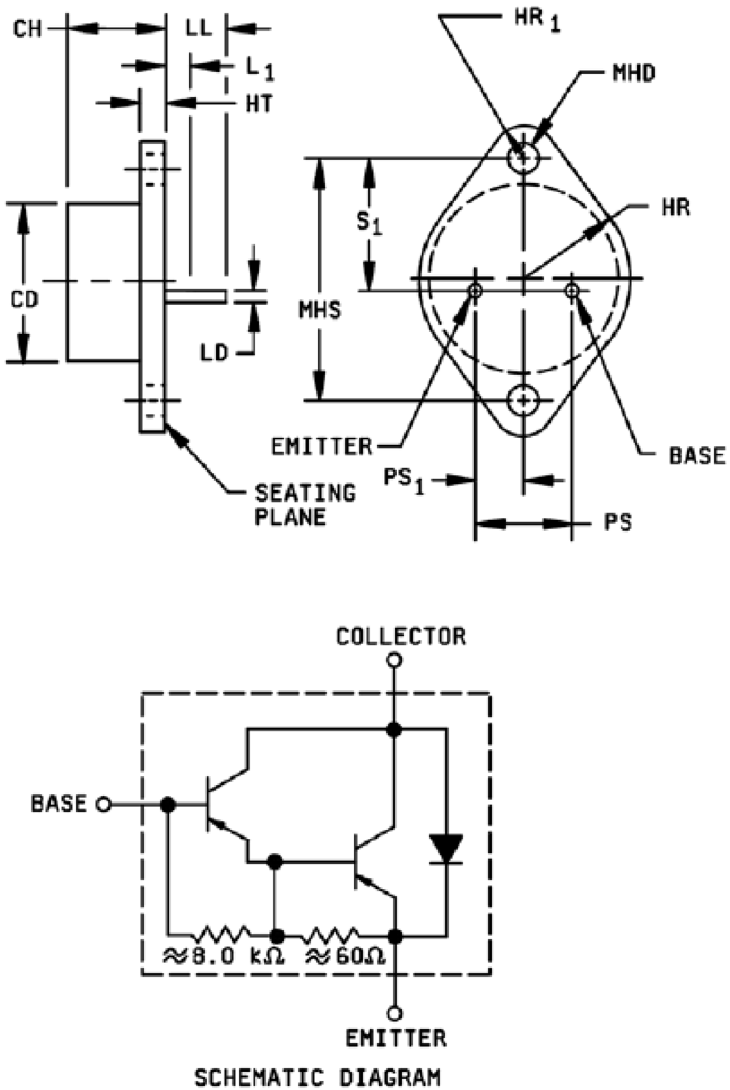


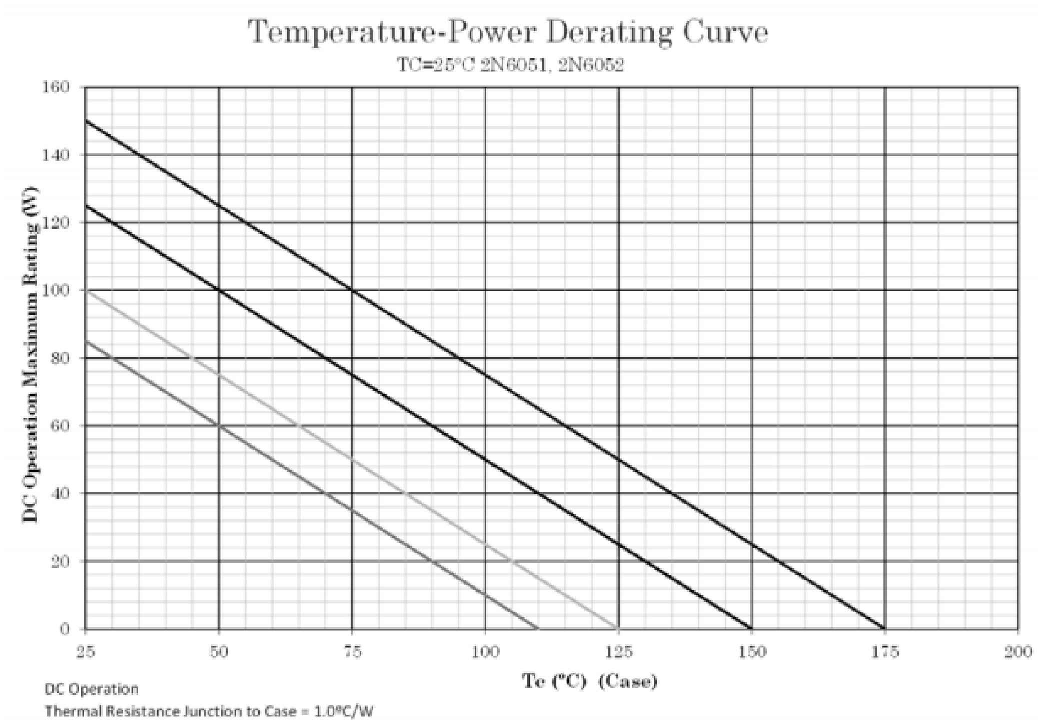

FIGURE 1. Physical dimensions (TO-3) and schematic circuit.

### Outline Drawing (TO-3)

| Ltr | Dimensions | | | | Notes |
|---|---|---|---|---|---|
| | Inches | | Millimeters | | |
| | Min | Max | Min | Max | |
| CD | | .875 | | 22.23 | 3 |
| CH | .250 | .328 | 6.35 | 8.33 | |
| HR | .495 | .525 | 12.57 | 13.34 | |
| $HR_1$ | .131 | .188 | 3.33 | 4.78 | 6 |
| HT | .060 | .135 | 1.52 | 3.43 | |
| LD | .038 | .043 | 0.97 | 1.09 | 4, 5, 9 |
| LL | .312 | .500 | 7.92 | 12.70 | 4, 5, 9 |
| $L_1$ | | .050 | | 1.27 | 5, 9 |
| MHD | .151 | .161 | 3.84 | 4.09 | 7 |
| MHS | 1.177 | 1.197 | 29.90 | 30.40 | |
| PS | .420 | .440 | 10.67 | 11.18 | |
| $PS_1$ | .205 | .225 | 5.21 | 5.72 | 5 |
| $S_1$ | .655 | .675 | 16.64 | 17.15 | |

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Body contour is optional within zone defined by CD.
4. These dimensions shall be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement shall be made at seating plane.
5. Both terminals.
6. At both ends.
7. Two holes.
8. The collector shall be electrically connected to the case.
9. LD applies between $L_1$ and LL. Lead diameter shall not exceed twice LD within $L_1$.
10. The seating plane of the header shall be flat within .001 inch (0.03 mm), concave to .004 inch (0.10 mm), convex inside a .930 inch (23.62 mm) diameter circle on the center of the header, and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm), convex overall.
11. In accordance with ASME Y14.5M, diameters are equivalent to $\phi$x symbology.

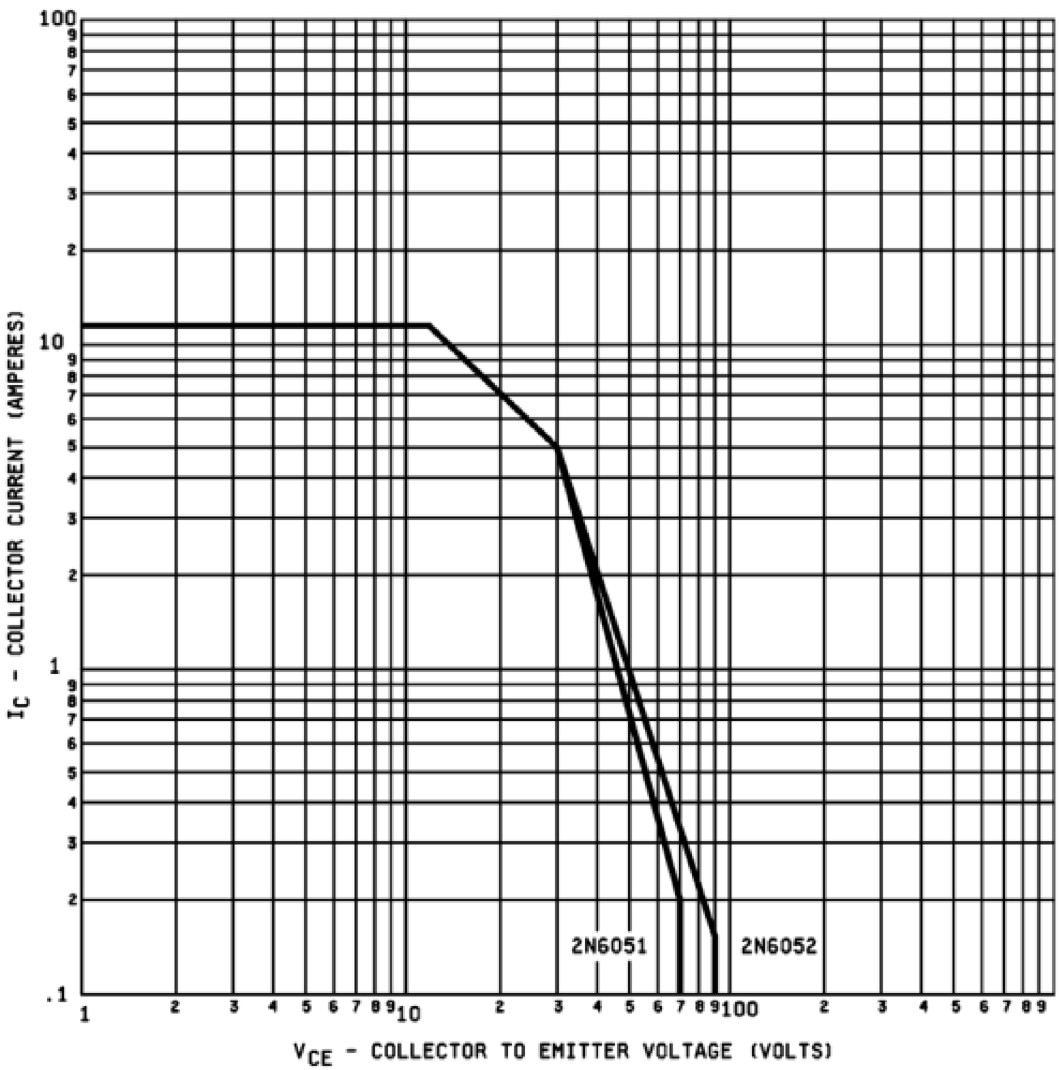
FIGURE 1. Physical dimensions (TO-3) and schematic circuit - Continued.




NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ $T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum $T_J$ allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J$ ≤ 175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J$ ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J$ ≤ 125°C, and 110°C to show power rating where most users want to limit $T_J$ in their application.

FIGURE 2. Temperature-power derating for 2N6051 AND 2N6052.


IC - COLLECTOR CURRENT (AMPERES)
VCE - COLLECTOR TO EMITTER VOLTAGE (VOLTS)
2N6051
2N6052

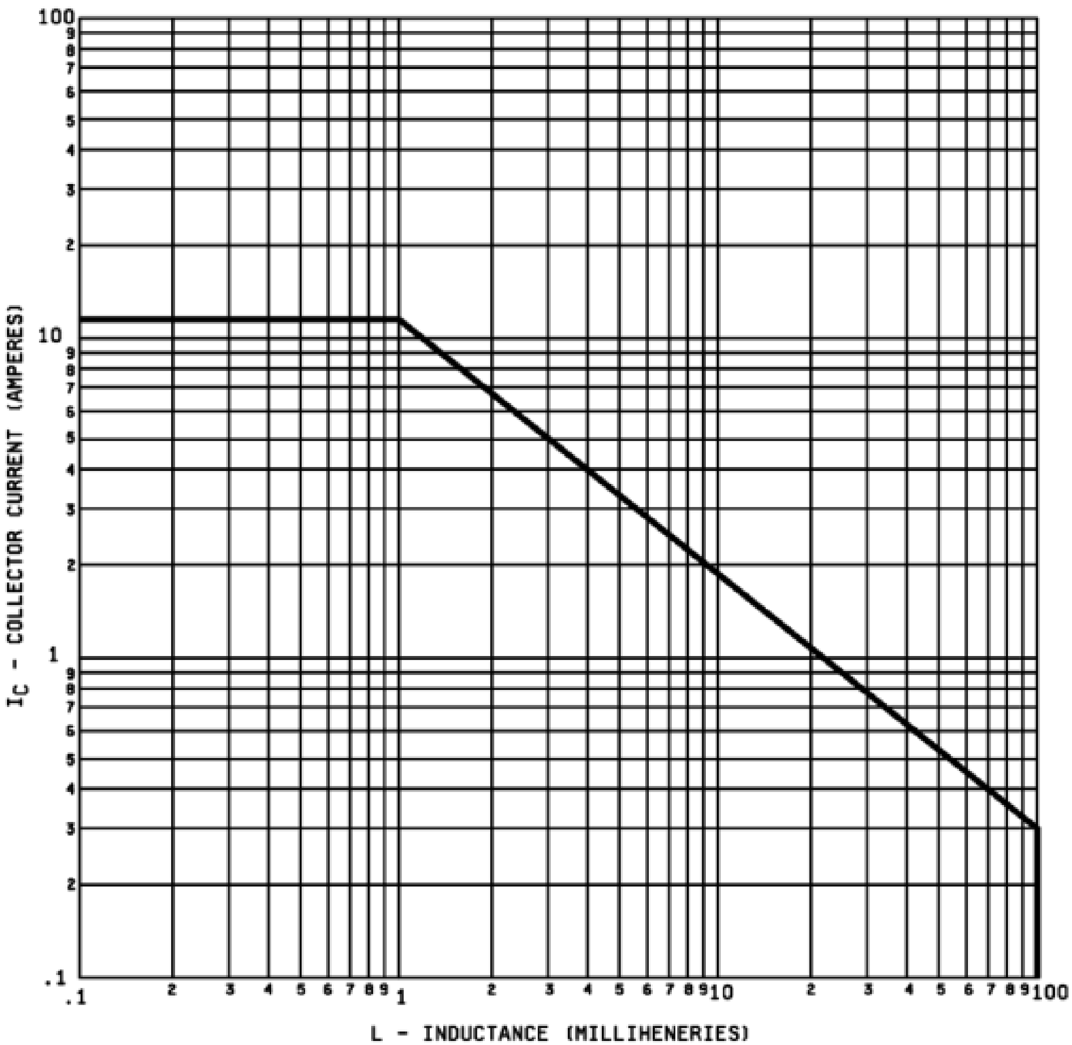



FIGURE 5. Safe operating area for switching between saturation and cutoff (unclamped inductive load).