DATA SHEET

Power Your Critical Mission Today

SVLFL5000D SERIES

SPACE QUALIFIED HYBRID DC-DC CONVERTERS

SVLFL – Exact marking may differ from that shown

Models Available
Input: 30 V to 60 V continuous, 80 V transient
Dual outputs: ±5 V, ±12 V, or ±15 V
Wattage: 100 W
MIL-PRF-38534: Class H and Class K; RHA level L

1.0 DESCRIPTION

The SVLFL Series of space qualified DC-DC converters is specifically designed for the harsh radiation environment of space applications. Performance is guaranteed through the use of hardened semiconductor components, radiation lot acceptance testing (RLAT) of non-hardened components, and analysis. The SVLFL Series has been characterized for Total Ionizing Dose (TID) performance including Enhanced Low Dose Rate Sensitivity (ELDRS) and for Single Event Effects (SEE) according to VPT's DLA-approved Radiation Hardness Assurance (RHA) plan per MIL-PRF-38534, Appendix G, Level L. Characterization is performed at both the component level and at the SVLFL Series hybrid converter level.

Radiation-hardened to TID levels of 60 krad(Si) and SEE to 85 MeV/mg/cm^2, the SVLFL Series of DC-DC converters is suited for use in many low Earth orbit (LEO), medium Earth orbit (MEO), geostationary orbit (GEO), deep space, and launch vehicle programs.

1.1 FEATURES

- Up to 100 W output power
- Wide input voltage range: 30 V to 60 V plus 80 V transient
- Continuous operation over full military temperature range of -55 °C to +125 °C with no power derating
- Very low output noise
- Parallel up to 4 units with current sharing
- Output voltage trim up +10% or down -20%
- Radiation immune magnetic feedback circuit
- No use of optoisolators
- Undervoltage lockout
- Current limit protection / short circuit protection

1.2 SPACE LEVEL CHARACTERIZATIONS

- Guaranteed TID performance to 60 krad(Si) including LDR
- SEE performance to 85 MeV/mg/cm^2. Transients are fully characterized for cross section and magnitude
- Worst-case analysis, stress, radiation, reliability reports available

1.3 MANUFACTURING AND COMPLIANCE

- Qualified to MIL-PRF-38534 Class H and Class K, DLA SMD # 5962-23212
- MIL-PRF-38534 element evaluated components
- MIL-STD-461 C/D/E/F when used with appropriate VPT EMI filter
- Manufactured in an ISO9001, MIL-PRF-38534 Class H and Class K facility
- MIL-STD-883

1.4 PACKAGING

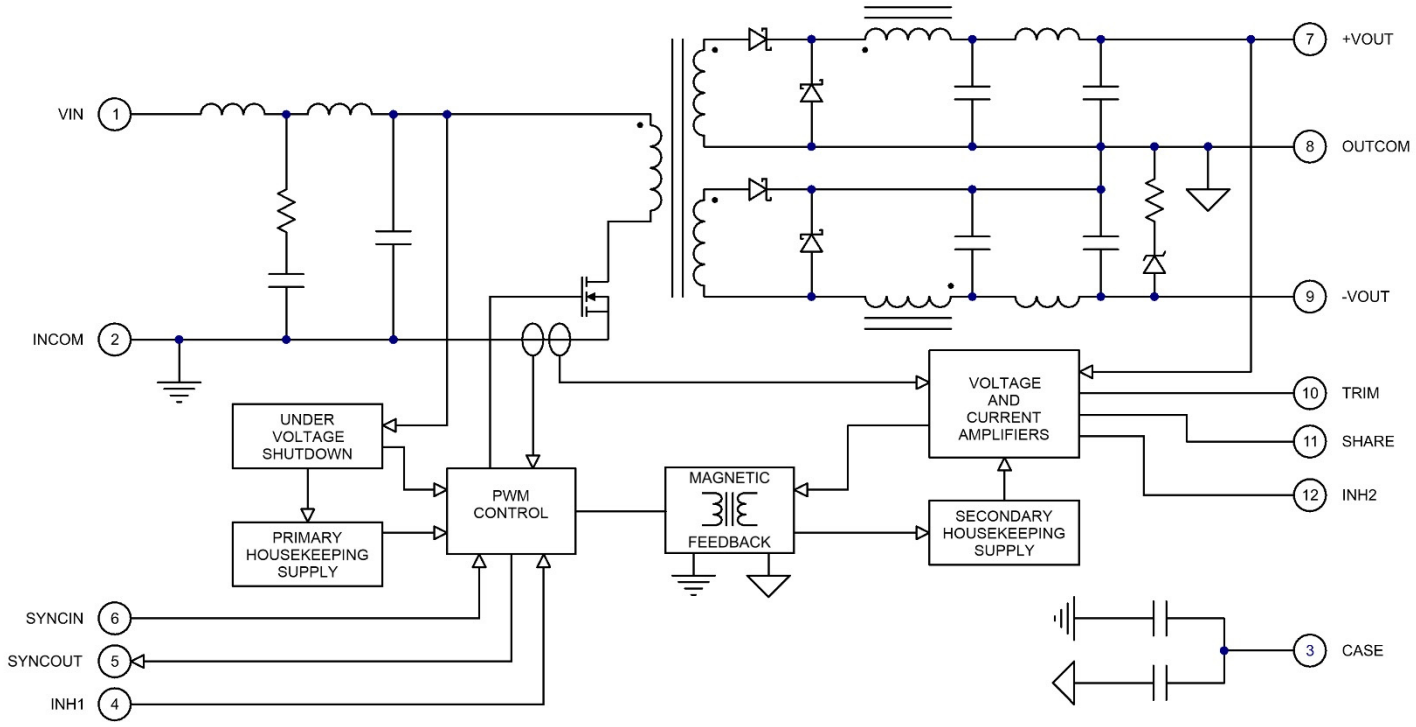
- Low-profile: 3.005" x 1.505" x 0.400"
- Max weight: 88 g
- Industry standard pinout
- Precision seam-welded hermetic metal case
- Standard and optional side-flanged versions available

1.5 ACCESSORIES

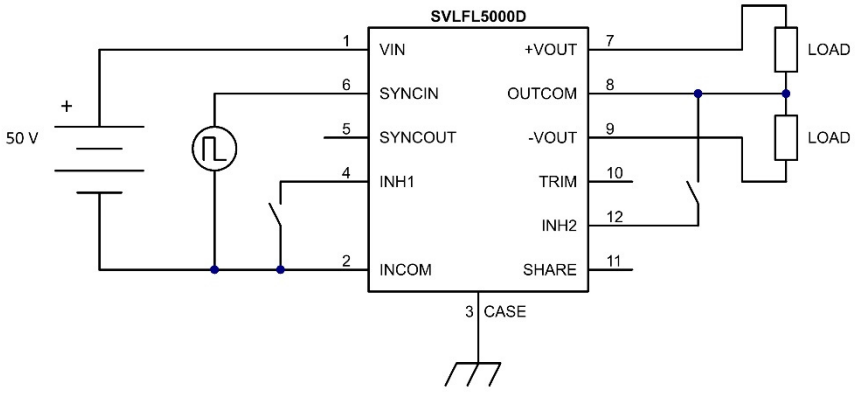
- EMI filters
- Use with Thermal Pad TP-001
- See www.vptpower.com for more information

2.0 DIAGRAMS

2.1 BLOCK DIAGRAM



2.2 CONNECTION DIAGRAM



3.0 SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings			
Input Voltage (Continuous):	-0.5 V to 60 V	Operating Temperature (Full Load):	-55 °C to +125 °C
Input Voltage (Transient, 1 second):	-0.5 V to 80 V	Storage Temperature:	-65 °C to +150 °C
ESD Rating per MIL-PRF-38534:	3B	Lead Solder Temperature (10 seconds):	270 °C

3.2 PERFORMANCE SPECIFICATIONS

Tcase = -55 °C to +125 °C, Vin = +50 V ± 5%, Full Load[1], Unless Otherwise Specified

		SVLFL5005D			SVLFL5012D			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
INPUT								
Voltage	Continuous	30	50	60	30	50	60	V
	Transient, 1 sec[4]	-	-	80	-	-	80	V
Current	INH 1 < 1.5 V	-	3	5	-	3	5	mA
	INH 2 < 1 V	-	40	70	-	40	70	mA
	No Load	-	60	100	-	65	110	mA
Ripple Current	20 Hz to 10 MHz	-	50	100	-	55	100	mApp
Undervoltage Lockout	Turn-On	26.5	28	29	26.5	28	29	V
	Turn-Off[4]	25.5	-	28.5	25.5	-	28.5	V
OUTPUT STATIC								
Voltage	+Vout, Tcase = 25 °C	4.95	5	5.05	11.88	12	12.12	V
	+Vout, Tcase = -55 °C to +125 °C	4.90	5	5.10	11.76	12	12.24	V
	-Vout, Tcase = 25 °C	4.85	5	5.15	11.76	12	12.24	V
	-Vout, Tcase = -55 °C to +125 °C	4.80	5	5.20	11.64	12	12.36	V
Power[2,6]	Total	0	-	100	0	-	100	W
	Either Output	0	-	70	0	-	70	W
Current[2,6]	Total	0	-	20	0	-	8.33	A
	Either Output	0	-	14	0	-	5.83	A
Ripple Voltage	20 Hz to 10 MHz	-	40	80	-	50	80	mVpp
Line Regulation	+Vout, V_{IN} = 30 V to 60 V	-	1	20	-	1	20	mV
	-Vout, V_{IN} = 30 V to 60 V	-	10	50	-	10	50	mV
Load Regulation[7]	+Vout, No Load to Full Load	-	10	100	-	10	150	mV
	-Vout, No Load to Full Load	-	100	200	-	50	200	mV
Cross Regulation, -Vout	+Vout: 30% load, -Vout: 70% load +Vout: 70% load, -Vout: 30% load	-	250	450	-	210	450	mV
Load Fault Power Dissipation[4]	Overload	-	-	50	-	-	50	W
	Short Circuit	-	-	50	-	-	50	W
OUTPUT DYNAMIC								
Load Step, Half to Full Load, Either Output	Output Transient	-	200	400	-	550	750	mVpk
	Recovery[3]	-	300	500	-	350	550	µs
Line Step[4], Vin = 30 V to 60 V	Output Transient	-	150	500	-	500	1200	mVpk
	Recovery[3]	-	300	500	-	300	500	µs
Turn-On, Vin = 0 V to 50 V	Delay	-	3	20	-	3	20	ms
	Overshoot	-	1	25	-	10	50	mVpk
FUNCTION								
INH 1 Pin Input[4]	Output Inhibited	0	-	1.5	0	-	1.5	V
INH 2 Pin Input[4]	Output Inhibited	0	-	1	0	-	1	V
INH 1 Pin Open Circuit Voltage[4]	Output Enabled	10.5	-	16	10.5	-	16	V
INH 2 Pin Open Circuit Voltage[4]	Output Enabled	4	-	12	4	-	12	V
Voltage Trim Range		-20	-	+10	-20	-	+10	%
SHARE Pin Voltage[4]		1.5	2.5	4	1.5	2.5	4	V
SYNC Frequency Range		500	-	600	500	-	600	kHz

1. Half load at +Vout and half load at -Vout.
2. Up to 70% of the total power or current can be drawn from either of the two outputs.
3. Time for output voltage to settle within 1% of steady-state value.
4. Verified by initial electrical design verification. Post design verification, parameter shall be guaranteed to the limits specified.
5. End-of-Life performance includes aging and radiation degradation and is within standard limits except where noted.
6. Derate linearly to 0 at 135 °C.
7. 5% load to full load at -55 °C.

3.2 PERFORMANCE SPECIFICATIONS (CONTINUED)

Tcase = -55 °C to +125 °C, Vin = +50 V ± 5%, Full Load[1], Unless Otherwise Specified

		SVLFL5005D			SVLFL5012D			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
GENERAL								
Efficiency		78	82	-	84	88	-	%
Capacitive Load[4]		-	-	500	-	-	500	µF
Switching Frequency		450	525	550	450	525	550	kHz
Isolation	500 V DC, Tcase = 25 °C	100	-	-	100	-	-	MΩ
Weight	Standard and optional side-flanged	-	-	88	-	-	88	g
MTBF (MIL-HDBK-217F) [8]	Class H, SF @ Tcase = 55 °C	-	690	-	-	690	-	khr
	Class K, SF @ Tcase = 55 °C	-	2.76	-	-	2.76	-	Mhr
POST-RAD END-OF-LIFE LIMITS[5]								
Input Ripple Current		-	-	120	-	-	120	mApp
Switching Frequency		435	-	575	435	-	575	kHz
Output Voltage	+Vout, Tcase = -55 °C to +125 °C	4.85	-	5.15	11.70	-	12.30	V
	-Vout, Tcase = -55 °C to +125 °C	4.75	-	5.25	11.52	-	12.48	V

1. Half load at +Vout and half load at -Vout.
2. Up to 70% of the total power or current can be drawn from either of the two outputs.
3. Time for output voltage to settle within 1% of steady-state value.
4. Verified by initial electrical design verification. Post design verification, parameter shall be guaranteed to the limits specified.
5. End-of-Life performance includes aging and radiation degradation and is within standard limits except where noted.
6. Derate linearly to 0 at 135 °C.
7. 5% load to full load at -55 °C.
8. Correction factor of 0.12 added to ceramic capacitors.

3.2 PERFORMANCE SPECIFICATIONS (CONTINUED)

Tcase = -55 °C to +125 °C, Vin = +50 V ± 5%, Full Load[1], Unless Otherwise Specified

		SVLFL5015D			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Units**
INPUT					
Voltage	Continuous	30	50	60	V
	Transient, 1 sec[4]	-	-	80	V
Current	INH 1 < 1.5 V	-	3	5	mA
	INH 2 < 1 V	-	40	70	mA
	No Load	-	90	120	mA
Ripple Current	20 Hz to 10 MHz	-	50	100	mApp
Undervoltage Lockout	Turn-On	26.5	28	29	V
	Turn-Off[4]	25.5	-	28.5	V
OUTPUT STATIC					
Voltage	+Vout, Tcase = 25 °C	14.85	15	15.15	V
	+Vout, Tcase = -55 °C to +125 °C	14.70	15	15.30	V
	-Vout, Tcase = 25 °C	14.70	15	15.30	V
	-Vout, Tcase = -55 °C to +125 °C	14.55	15	15.45	V
Power[2,6]	Total	0	-	100	W
	Either Output	0	-	70	W
Current[2,6]	Total	0	-	6.67	A
	Either Output	0	-	4.67	A
Ripple Voltage	20 Hz to 10 MHz	-	30	80	mVpp
Line Regulation	+Vout, V_{IN} = 30 V to 60 V	-	1	20	mV
	-Vout, V_{IN} = 30 V to 60 V	-	30	100	mV
Load Regulation[7]	+Vout, No Load to Full Load	-	10	150	mV
	-Vout, No Load to Full Load	-	50	250	mV
Cross Regulation, -Vout	+Vout: 30% load, -Vout: 70% load	-	200	450	mV
	+Vout: 70% load, -Vout: 30% load				
Load Fault Power Dissipation[4]	Overload	-	-	50	W
	Short Circuit	-	-	50	W
OUTPUT DYNAMIC					
Load Step, Half to Full Load, Either Output	Output Transient	-	450	700	mVpk
	Recovery[3]	-	200	500	µs
Line Step[4], Vin = 30 V to 60 V	Output Transient	-	500	1200	mVpk
	Recovery[3]	-	300	500	µs
Turn-On, Vin = 0 V to 50 V	Delay	-	3	20	ms
	Overshoot	-	10	50	mVpk
FUNCTION					
INH 1 Pin Input[4]	Output Inhibited	0	-	1.5	V
INH 2 Pin Input[4]	Output Inhibited	0	-	1	V
INH 1 Pin Open Circuit Voltage[4]	Output Enabled	10.5	-	16	V
INH 2 Pin Open Circuit Voltage[4]	Output Enabled	4	-	12	V
Voltage Trim Range		-20	-	+10	%
SHARE Pin Voltage[4]		1.5	2.5	4	V
SYNC Frequency Range		500	-	600	kHz

1. Half load at +Vout and half load at -Vout.
2. Up to 70% of the total power or current can be drawn from either of the two outputs.
3. Time for output voltage to settle within 1% of steady-state value.
4. Verified by initial electrical design verification. Post design verification, parameter shall be guaranteed to the limits specified.
5. End-of-Life performance includes aging and radiation degradation and is within standard limits except where noted.
6. Derate linearly to 0 at 135 °C.
7. 5% load to full load at -55 °C.

3.2 PERFORMANCE SPECIFICATIONS (CONTINUED)

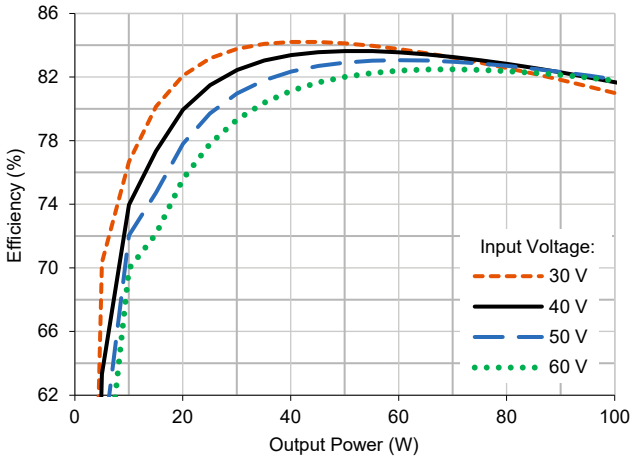
Tcase = -55 °C to +125 °C, Vin = +50 V ± 5%, Full Load[1], Unless Otherwise Specified

		SVLFL5015D			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Units**
GENERAL					
Efficiency		78	86	-	%
Capacitive Load[4]		-	-	500	µF
Switching Frequency		450	525	550	kHz
Isolation	500 V DC, Tcase = 25 °C	100	-	-	MΩ
Weight	Standard and optional side-flanged	-	-	88	g
MTBF (MIL-HDBK-217F) [8]	Class H, SF @ Tcase = 55 °C	-	690	-	kHr
	Class K, SF @ Tcase = 55 °C	-	2.76	-	Mhr
POST-RAD END-OF-LIFE LIMITS[5]					
Input Ripple Current		-	-	120	mApp
Switching Frequency		435	-	575	kHz
Output Voltage	+Vout, Tcase = -55 °C to +125 °C	14.600	-	15.375	V
	-Vout, Tcase = -55 °C to +125 °C	14.400	-	15.600	V

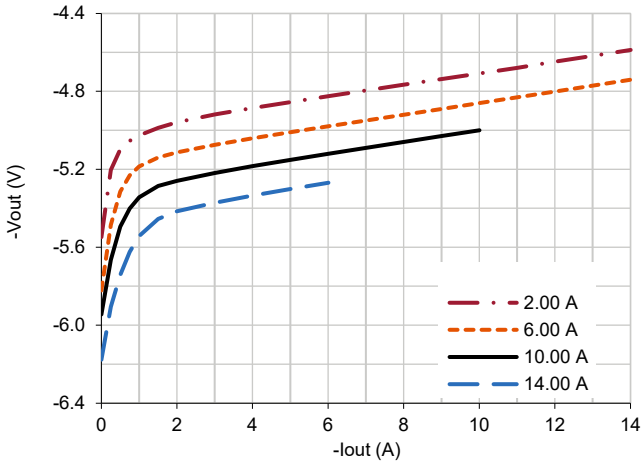
1. Half load at +Vout and half load at -Vout.
2. Up to 70% of the total power or current can be drawn from either of the two outputs.
3. Time for output voltage to settle within 1% of steady-state value.
4. Verified by initial electrical design verification. Post design verification, parameter shall be guaranteed to the limits specified.
5. End-of-Life performance includes aging and radiation degradation and is within standard limits except where noted.
6. Derate linearly to 0 at 135 °C.
7. 5% load to full load at -55 °C.
8. Correction factor of 0.12 added to ceramic capacitors.

4.0 PERFORMANCE CURVES

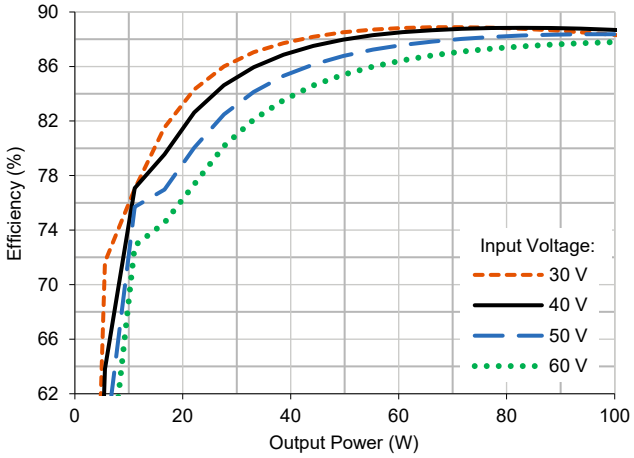
4.1.1 SVLFL5005D Efficiency (Typical, 25 °C)



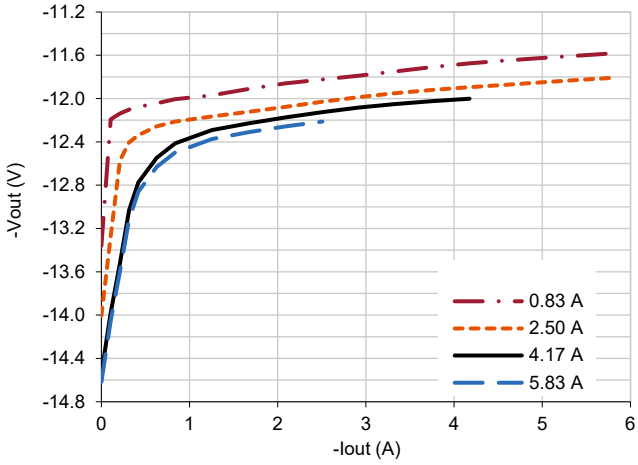
4.1.2 SVLFL5005D Cross-Regulation (Typical, 25 °C)



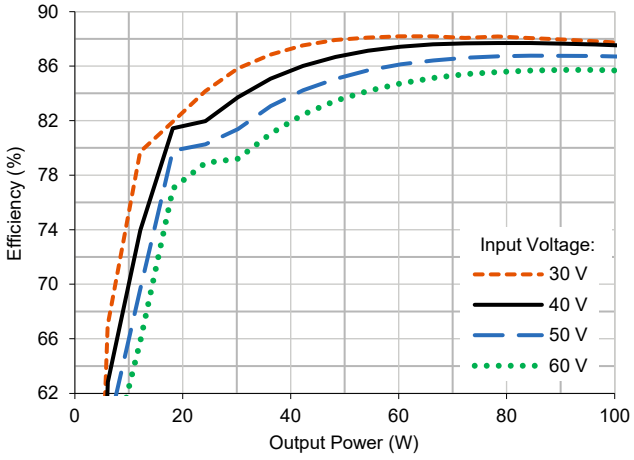
4.2.1 SVLFL5012D Efficiency (Typical, 25 °C)



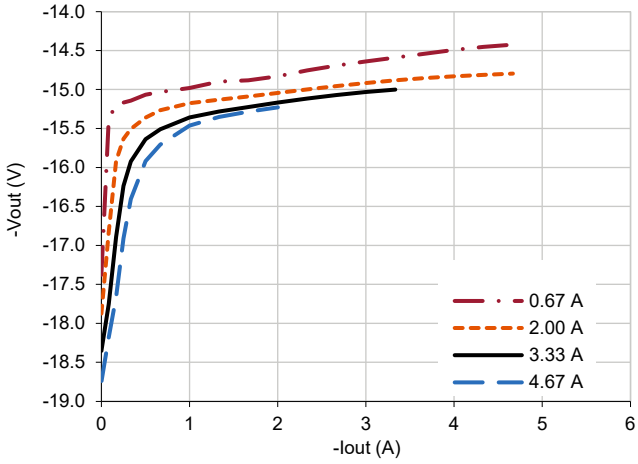
4.2.2 SVLFL5012D Cross-Regulation (Typical, 25 °C)



4.3.1 SVLFL5015D Efficiency (Typical, 25 °C)

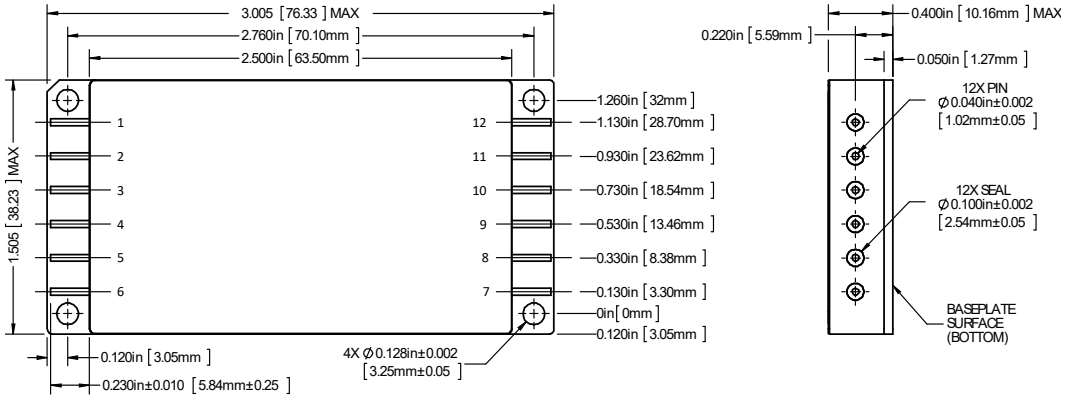


4.3.2 SVLFL5015D Cross-Regulation (Typical, 25 °C)



5.0 MECHANICAL OUTLINES AND PINOUT

Standard Package:

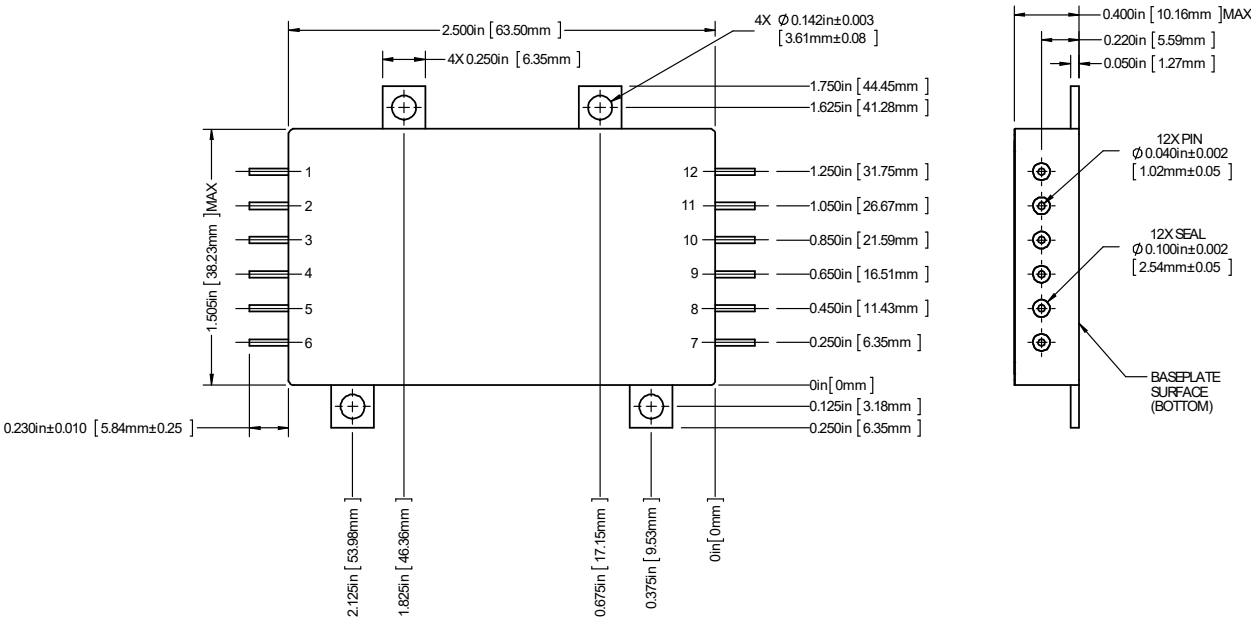


1. Tolerances are ±0.005" unless otherwise stated.
2. Case temperature is measured on the center of the baseplate surface.
3. Mounting holes are not threaded. Recommended fastener is #4-40 screw.
4. Materials: Case (Steel, gold over nickel plated); Cover (Kovar, nickel plated); Pin (Copper-cored alloy 52, gold over nickel plated); Pin Seals (Glass).

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	50VIN	4	INH1	7	+VOUT	10	TRIM
2	INCOM	5	SYNCOUT	8	OUTCOM	11	SHARE
3	CASE	6	SYNCIN	9	-VOUT	12	INH2

5.0 MECHANICAL OUTLINES AND PINOUT (CONTINUED)

Optional Side-Flanged Package:



1. Tolerances are ±0.005" unless otherwise stated.
2. Case temperature is measured on the center of the baseplate surface.
3. Mounting holes are not threaded. Recommended fastener is #4-40 screw.
4. Materials: Case (Steel, gold over nickel plated); Cover (Kovar, nickel plated); Pin (Copper-cored alloy 52, gold over nickel plated); Pin Seals (Glass).

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	50VIN	4	INH1	7	+VOUT	10	TRIM
2	INCOM	5	SYNCOUT	8	OUTCOM	11	SHARE
3	CASE	6	SYNCIN	9	-VOUT	12	INH2

6.0 TECHNICAL NOTES

Please note that many of these functions are also demonstrated in detail on the VPT website in the form of technical video labs.

6.1 GENERAL INFORMATION

6.1.1 Topology Description

The SVLFL5000D Series is an isolated, dual-output, forward converter. It provides a positive and negative output voltage with respect to the OUTCOM pin. Up to 70% of the total output power is available from either output. The internal voltage regulation loop actively regulates the positive output using VPT's proprietary magnetic feedback technology. The negative output is regulated by cross-regulation. The negative output is well-regulated for balanced load conditions. For unbalanced load conditions, refer to the cross regulation performance graphs in Section 4.0 for expected performance. For a balanced or near-balanced load condition, the converter will regulate down to zero load, and no minimum load is required. For an unbalanced load condition, with negative loads greater than 10%, a minimum load of 10% is recommended on the positive output.

6.1.2 External Components

The SVLFL5000D Series is designed to operate stand-alone in most applications. It does not require any external components for proper operation or to meet the datasheet specifications. Input and output L-C filters are provided internally for low ripple and noise. To further reduce output ripple and noise, a small ceramic capacitor, 1 µF to 10 µF, can be added at the output. Most application specific ripple requirements can be met with the addition of output capacitors alone. External output capacitance can be added up to the maximum listed in Section 3.2.

6.1.3 Source Impedance

The impedance of the 50 V input source can interact with the DC-DC converter and can affect performance. High source impedance is often caused by a long input cable or components added in series with the input. Source resistance will cause a DC voltage drop as the converter draws DC input current. This voltage drop is simply the cable resistance multiplied by the input current at low line. The voltage drop and the actual voltage at the input to the converter will determine the minimum source voltage at which the converter will operate. A high source inductance can interact with the feedback control loop of the converter. VPT's EMI filters will usually isolate the source and eliminate this problem. In some cases, additional input capacitance will be needed to stabilize the system.

6.1.4 Output Configurations

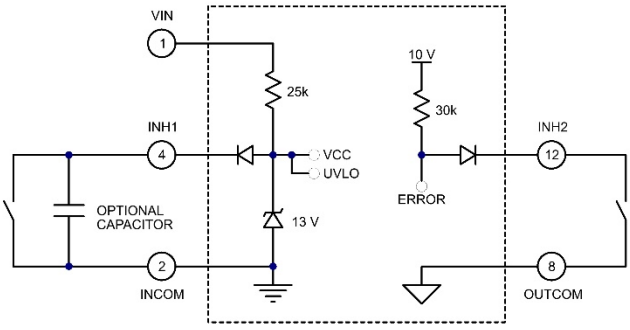
Since the converter is isolated, the outputs can be used as a traditional dual-output, with a positive and negative voltage referenced to OUTCOM, or as a single-ended output referenced to -VOUT or +VOUT. For example, the SVLFL5012D model can provide +12 V and -12 V in the traditional dual output configuration, or can provide +24 V referenced to -VOUT, or -24 V referenced to +VOUT in single-ended configuration. In the single-ended configuration, the OUTCOM pin will be at +12 V relative to -VOUT.

The outputs of multiple converters can be stacked in series to provide higher voltages. When outputs of multiple modules are stacked, they naturally share the load. For example, two SVLFL5012D converters can be stacked to provide a 48 V output at 200 W.

6.2 FUNCTION DESCRIPTIONS

6.2.1 On/Off Control (INH1 and INH2)

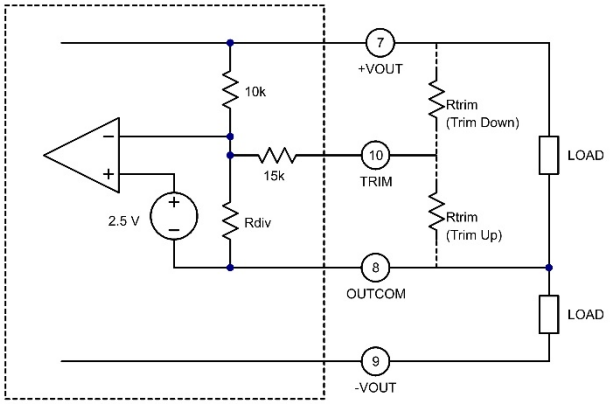
The INH1 (Inhibit 1) pin is a primary-side control pin referenced to INCOM. The INH1 pin must be driven using an open collector or open drain configuration. Pulling the INH1 pin low disables the converter output, removes bias voltage from internal control circuitry, and puts the converter in a state of minimum input current draw. Leaving INH1 open enables the output, allowing the converter to operate normally. The pin must be pulled below 1.5 V to disable the output. An optional capacitor from INH1 to INCOM may be used to delay turn-on. The INH1 pin should be left open if not used.



The INH2 (Inhibit 2) pin is a secondary-side control pin referenced to OUTCOM. The INH2 pin must also be driven in an open collector or open drain configuration. Pulling INH2 low to OUTCOM disables the converter output. Internal control circuits, however, remain active. The pin must be pulled below 1.0 V to disable the output. The INH2 pin should be left open if not used.

6.2.2 Adjusting the Output Voltage (TRIM)

The output voltage set point of the converter can be adjusted using the TRIM pin. To adjust the output up, connect the trim resistor from TRIM to OUTCOM. To adjust the output down, connect the trim resistor from TRIM to +VOUT. The maximum trim range is -20% and +10% from nominal. The appropriate resistor values versus the output voltage are given in the table below. Because the TRIM pin can be sensitive to external noise, the trim resistor should be physically located close to the SVLFL converter with short interconnects. The TRIM pin should be left open if not used. When adjusting the output voltage, do not exceed the rated total output power or output current.



SVLFL5005D		SVLFL5012D		SVLFL5015D	
+Vout (V)	Rtrim (Ω)	+ Vout (V)	Rtrim (Ω)	+ Vout (V)	Rtrim (Ω)
5.5	35.0k	13.2	5.80k	16.50	1.70k
5.4	47.5k	13.0	10.0k	16.25	5.00k
5.3	68.3k	12.8	16.2k	16.00	10.0k
5.2	110k	12.6	26.6k	15.75	18.3k
5.1	235k	12.4	47.3k	15.50	35.0k
5.0	—	12.2	109k	15.25	85.0k
4.9	225k	12.0	—	15.00	—
4.8	100k	11.8	454k	14.75	475k
4.7	58.3k	11.6	213k	14.50	225k
4.6	37.5k	11.4	134k	14.25	142k
4.5	25.0k	11.2	94.0k	14.00	100k
4.4	16.7k	11.0	70.1k	13.75	75.0k
4.3	10.7k	10.8	54.3k	13.50	58.3k
4.2	6.30k	10.6	42.9k	13.25	46.4k
4.1	2.80k	10.4	34.4k	13.00	37.5k
4.0	short	10.2	27.8k	12.75	30.6k
		10.0	22.5k	12.50	25.0k
		9.8	18.2k	12.25	20.5k
		9.6	14.6k	12.00	16.7k

6.2.3 Frequency Synchronization (SYNCIN, SYNCOUT)

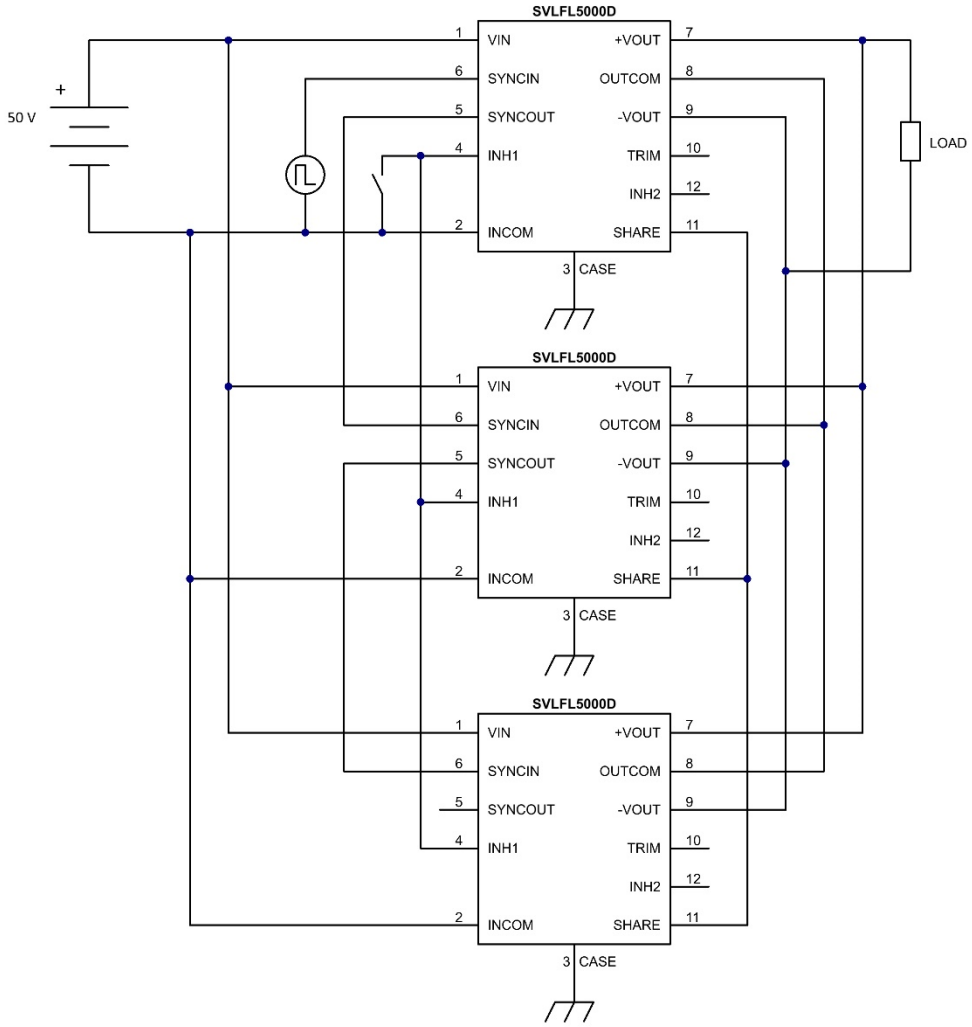
The SVLFL5000D Series will free run at a switching frequency of approximately 525 kHz, which has been set for optimum converter performance. Frequency synchronization is not necessary unless required by system constraints. The SVLFL5000D Series provides a frequency synchronization input (SYNCIN) and output (SYNCOUT), both referenced to INCOM.

The SYNCIN pin can be driven by an external clock or by the SYNCOUT pin of another SVLFL converter. The internal clock and internal power train will operate at the frequency applied to the SYNCIN pin. The SYNCIN pin should be driven with a TTL type 5 V square wave signal. The duty cycle of the square wave should be between 20% and 80%. The SYNCIN pin is internally capacitively-coupled and the internal load is equivalent to 220 pF. Proper layout and circuit techniques are necessary to prevent noise from being injected into this pin. Synchronized converters should be located physically close together and share a low impedance INCOM connection. The SYNCIN pin can be left open or connected to INCOM if not used.

The SYNCOUT pin provides a 5 V quasi-square wave output at either the SYNCIN frequency or the free-running frequency if SYNCIN is not used. The SYNCOUT of a SVLFL can be connected to the SYNCIN pin of a second SVLFL to synchronize its switching frequency to that of the first SVLFL. Similarly, the SYNCOUT of the second SVLFL can be connected to SYNCIN of a third SVLFL. Subsequent SVLFL converters can be connected in this daisy chain arrangement as shown in the figure in section 6.2.4. SYNCOUT should be left open if not used.

6.2.4 Parallel Operation (SHARE)

The SVLFL5000D Series provides a SHARE function for active current sharing among paralleled modules. For the dual output model, the SHARE function is only applicable in the single-ended output configuration (see section 6.1.4) where no current is drawn from the OUTCOM pin. To enable load sharing, connect a single wire between the SHARE pins of all parallel modules. The SHARE pin can be noise sensitive. Paralleled converters should be located physically close to one another and share a low impedance OUTCOM connection. A symmetrical layout of the output traces will improve share accuracy. Frequency synchronization is not required for parallel operation. The SHARE pin should be left open if not used.



6.3 PROTECTION FEATURES

6.3.1 Input Undervoltage Lockout

The SVLFL5000D Series provides input undervoltage lockout protection. For input voltages below the turn-on voltage, the converter will remain off, drawing minimal current from the source. When the input voltage exceeds the turn-on voltage, the converter will start. The lockout circuit is designed to tolerate slow ramping input voltage waveforms. VPT's proprietary magnetic feedback technology provides bias voltage to all secondary control circuits and control amplifiers before the output starts, ensuring a well-controlled start up sequence.

6.3.2 Output Soft Start

The SVLFL5000D Series utilizes an output soft-start function to ramp the output in a controlled manner, eliminating output voltage overshoot and limiting inrush current at turn on. A voltage-mode soft-start ensures the output waveform remains consistent regardless of changes in the load current. The output rise time is approximately 3 ms. The soft-start function is active whether the module is turned on with an application of input voltage or from release of the inhibit pin. Under normal conditions, current drawn from the source during turn on will not exceed the full load input current. The turn-on delay time is specified from the application of input voltage (or release of the inhibit pin) until the output reaches 90% of its final value.

6.3.3 Output Overcurrent Protection

The SVLFL5000D Series provides output overcurrent and output short circuit protection. During a load fault condition, a constant output current control circuit reduces the converter duty cycle to limit the total output current to approximately 125% its rated value. The current limit protection circuit limits the sum of output currents in both +Vout and -Vout. It does not distinguish if the current is on the positive or negative output. The converter will continue to provide constant current into any overload or short circuit condition. This feature allows the converter to start into any capacitive load. Recovery is automatic and immediate upon removal of the fault condition. Sustained short circuit or overload operation can cause excessive power dissipation. Care should be taken to control the operating temperature of the converter in this condition.

6.4 THERMAL CONSIDERATIONS

The SVLFL5000D Series is rated for full power operation at 125 °C. Operation above 125 °C is allowed at reduced power. Specifically, the output power should be derated linearly from full power at 125 °C to half power at 130 °C and to zero power at 135 °C. The operating temperature of the converter is specified on the baseplate of the converter. The converter is designed to be conduction-cooled, with the baseplate mounted to a heat sink, chassis, PCB, or other thermal surface. The internal power dissipating components are mounted to the baseplate of the converter and all heat flow is through the baseplate and mounting flanges. The lid of the converter does not provide a good thermal path.

The hybrid DC-DC converter contains many semiconductor components. The maximum temperature rise from junction to case is 20 °C at full load.

6.5 VPT RHA PLAN AND APPROACH

VPT takes a conservative approach to radiation testing to ensure product performance in a space environment. VPT's DLA-approved Radiation Hardness Assurance (RHA) plan documents VPT's processes and procedures for guaranteeing the performance of VPT products under various environmental conditions in space including Total Ionizing Dose (TID) and Single-Event Effects (SEE). Additionally, Enhanced Low Dose-Rate Sensitivity (ELDRS) effects are considered for all bipolar ICs used in the hybrid. Hardness is guaranteed by a combination of both hybrid-level characterization and Radiation Lot Acceptance Testing (RLAT) of all sensitive semiconductor piece-parts used within the hybrid.

6.5.1 Radiation Test and Performance Levels

Radiation Environment		Piece Part RLAT	Hybrid-Level Characterization
Total Ionizing Dose (TID)	High Dose Rate (HDR)	60 krad(Si)	60 krad(Si)
	Low Dose Rate (LDR)	[1]60 krad(Si)	60 krad(Si)
Single-Event Effects (SEE)	Destructive (SEB, SEGR, SEL)	Not applicable	≥ 85 MeV/mg/cm^2
	Non-Destructive (SET, SEU)	Not applicable	≥ 85 MeV/mg/cm^2

1. Piece-part LDR screening performed only on potentially ELDRS parts (bipolar ICs).

6.5.2 RHA Plan Summary

Test	RHA Plan for SVL Series Isolated DC-DC Converters
Total Ionizing Dose (TID):	Sensitive semiconductor components undergo RLAT to 60 krad(Si) per MIL-STD-883 Method 1019. Converters are characterized to 60 krad(Si).
Enhanced Low Dose Rate Sensitivity (ELDRS):	All bipolar linear ICs are characterized for ELDRS and tested in accordance with MIL-STD-883 test method 1019 section 3.13
Single Event Effects (SEE):	Converters are characterized to LET ≥ 85 MeV/mg/cm^2 for both catastrophic events (SEL, SEB, SEGR) and functional interrupts (SEFI) under heavy ion exposure. Converters are also characterized for cross-section and magnitude of output transients (SET) for at least 3 different LET levels.
Radiation Lot Acceptance Testing (RLAT):	All production lots of sensitive semiconductor components undergo RLAT for TID at HDR and/or LDR as appropriate per part type.

6.5.3 RHA Designators available on SMD

The SVLFL5000D series converters are available on SMD with RHA level L. See section 8.0 for full SMD number information.

6.5.4 Supporting Documentation Available (Contact Sales)

Report	Description
Radiation Hardness Assurance Plan:	DLA-approved RHA plan covering TID, SEE, and ELDRS
Worst-Case Analysis Report:	Detailed worst-case analysis including electrical stress/derating limits and guaranteed circuit performance post-radiation and end of life
Radiation Test Summary Report:	Overview of piece-part RLAT and hybrid characterization for all guaranteed environments. Also includes SEE cross-section data.
Reliability Report:	MTBF report based on MIL-HDBK-217 reliability calculations.
Thermal Analysis Report:	Component temperature rise analysis and measurement results.

7.0 ENVIRONMENTAL SCREENING

100% tested per MIL-STD-883 as referenced to MIL-PRF-38534.

Contact sales for more information concerning additional environmental screening and testing options. VPT Inc. reserves the right to ship higher screened or SMD products to meet orders for lower screening levels at our sole discretion unless specifically forbidden by customer contract.

Test	MIL-STD-883 Test Method, Condition	/H+ (Class H Screening + PIND)	/K and /KL1[1,7] (Class K Screening)	/EM (Engineering Model, Non-QML[1,6])
Non-Destructive Bond Pull	TM2023	•[2]	•	•[2]
Internal Visual	TM2010, TM2017, TM2032 (MIL-STD-750, TM2072, TM2073)	•	•	•
Temperature Cycling	TM1010, Condition C -65 °C to 150 °C, Ambient	•	•	
Constant Acceleration	TM2001, 3000g, Y1 Direction	•	•	
PIND[3]	TM2020, Condition A	•[2]	•	
Pre Burn-In Electrical	25 °C		•	
Burn-In	TM1015, 320 hrs., 125 °C, Case Typ		•	
	TM1015, 160 hrs., 125 °C, Case Typ	•		
	24 hrs., 125 °C, Case Typ			•
Final Electrical	MIL-PRF-38534, Group A Subgroups 1-6 -55 °C, 25 °C, 125 °C[4]	•	•	
	MIL-PRF-38534, Group A Subgroups 1 and 4 25 °C			•
Hermeticity (Seal)	TM1014, Fine Leak, Condition A2 or B1	•	•	
	TM1014, Gross Leak, Condition C1 or B2	•	•	
	Gross Leak, Dip (No Bomb), Visual Verification			•
Radiography[5]	TM2012		•	
External Visual	TM2009	•	•	•

1. Non-QML products may not meet all requirements of MIL-PRF-38534.
2. Not required per MIL-PRF-38534. Test performed for additional product quality assurance.
3. PIND test Certificate of Compliance included in product shipment.
4. 100% R&R testing with all test data included in product shipment.
5. Radiographic test Certificate of Compliance and film(s) or data CD included in product shipment.
6. Engineering models utilize only the screening specified and are not considered compliant for flight use.
7. -KL1 products are identical in every way with Class K products in compliance with MIL-PRF-38534 revision L and later revisions except they contain elements evaluated to the requirements of MIL-PRF-38534 revision K and previous revisions. These devices are not marked with an SMD number or MIL-PRF-38534 certification mark and are marked with -KL1 screening code in place of -K.

8.0 STANDARD MICROCIRCUIT DRAWING (SMD) NUMBERS

Standard Microcircuit Drawing Number	SVLFL5000D Series Similar Part Number
5962L2321201HXC	SVLFL5005D/H+
5962L2321201HXA	SVLFL5005D/H+-E
5962L2321201HYC	SVLFL5005D/K
5962L2321201HYA	SVLFL5005D/K-E
5962L2321201KXC	SVLFL5005DF/H+
5962L2321201KXA	SVLFL5005DF/H+-E
5962L2321201KYC	SVLFL5005DF/K
5962L2321201KYA	SVLFL5005DF/K-E
5962L2321202HXC	SVLFL5012D/H+
5962L2321202HXA	SVLFL5012D/H+-E
5962L2321202HYC	SVLFL5012D/K
5962L2321202HYA	SVLFL5012D/K-E
5962L2321202KXC	SVLFL5012DF/H+
5962L2321202KXA	SVLFL5012DF/H+-E
5962L2321202KYC	SVLFL5012DF/K
5962L2321202KYA	SVLFL5012DF/K-E
5962L2321203HXC	SVLFL5015D/H+
5962L2321203HXA	SVLFL5015D/H+-E
5962L2321203HYC	SVLFL5015D/K
5962L2321203HYA	SVLFL5015D/K-E
5962L2321203KXC	SVLFL5015DF/H+
5962L2321203KXA	SVLFL5015DF/H+-E
5962L2321203KYC	SVLFL5015DF/K
5962L2321203KYA	SVLFL5015DF/K-E

Do not use the SVLFL5000D Series similar part number for SMD product acquisition. It is listed for reference only. For exact specifications for the SMD product, refer to the SMD drawing. SMDs can be downloaded from the DLA Land and Maritime (Previously known as DSCC) website at https://landandmaritimeapps.dla.mil/programs/defaultapps.asp. The SMD number listed above represents the Federal Stock Class, Device Type, Device Class Designator, Case Outline, Lead Finish and RHA Designator (where applicable). Please reference the SMD for other screening levels, lead finishes, and radiation levels. All SMD products are marked with a “Q” on the cover as specified by the QML certification mark requirement of MIL-PRF-38534.

9.0 ORDERING INFORMATION

SVLFL	50	05	D	F	/K	-	XXX
1	2	3	4	5	6		7

(1) Product Series	(2) Nominal Input Voltage	(3) Output Voltage	(4) Number of Outputs	(5) Package Option	(6) Screening Code[1,2,3,4]	(7) Additional Screening Code
SVLFL	**50** 50 V	**05** 5 V **12** 12 V **15** 15 V	**D** Dual	(None) Standard **F** Side-Flanged	**/EM** Engineering Model **/H+** Class H + PIND **/K** Class K **/KL1** Class K (KL1)	Contact Sales

1 Contact the VPT Sales Department for availability of Class H (/H) or Class K (/K) qualified products.
2 VPT Inc. reserves the right to ship higher screened or SMD products to meet lower screened orders at our sole discretion unless specifically forbidden by customer contract.
3 Engineering models utilize only the standard screening specified and are not considered compliant for flight use. These models are intended for low volume engineering characterization only and have no guarantee regarding operation in a radiation environment. The customer must place the following statement on each line item of their purchase order(s) for /EM units when ordering engineering models:

"(Customer Name) acknowledges that the /EM unit listed in this line item is not permitted for flight use and will be used for Engineering characterization only."

4. -KL1 products are identical in every way with Class K products in compliance with MIL-PRF-38534 revision L and later revisions except they contain elements evaluated to the requirements of MIL-PRF-38534 revision K and previous revisions. These devices are not marked with an SMD number or MIL-PRF-38534 certification mark and are marked with -KL1 screening code in place of -K.

Please contact your sales representative or the VPT Inc. Sales Department for more information concerning additional environmental screening and testing, different input voltage, output voltage, power requirements, source inspection, and/or special element evaluation for space or other higher quality applications.

10.0 CONTACT INFORMATION

To request a quotation or place orders please contact your sales representative or the VPT, Inc. Sales Department at:

Phone: (425) 353-3010
Fax: (425) 353-4030
E-mail: vptsales@vptpower.com

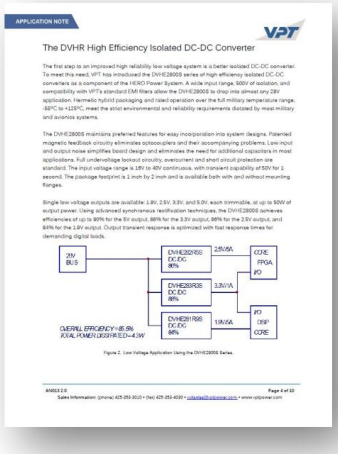
All information contained in this datasheet is believed to be accurate, however, no responsibility is assumed for possible errors or omissions. The products or specifications contained herein are subject to change without notice.

11.0 ADDITIONAL INFORMATION

Visit the VPT website for additional technical resources, including:

Product Catalogs

Application Notes and White Papers



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