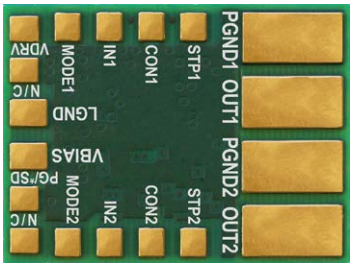
Features

- 10 A Fully De-Rated Operation Each Driver
- 100 V Fully De-Rated Operation (100 V Capable)
- **Dual Independent** Low-Side Power Switches
- 100 V HEMT Power Switches
- 100 V Schottky Catch Diodes
- Internal Power Good Circuitry
- Internal V_{BIAS} Overvoltage Protection
- Input Shoot-Through Protection
- High Speed Switching Capability: 3.0 MHz
- Rugged Compact Molded SMT Package
- "Pillar" I/O Pads
- Compact Size: 1.00 x 0.75 x 0.125"
- eGaN® Switching Elements
- Commercially Screened
- -40°C to +85°C Operational Range

Application

- High-Speed DC-DC Conversion
- Synchronous Rectification
- Multi-Phase Motor Drivers
- Power Switches/Actuators
- Commercial EPS & Avionics



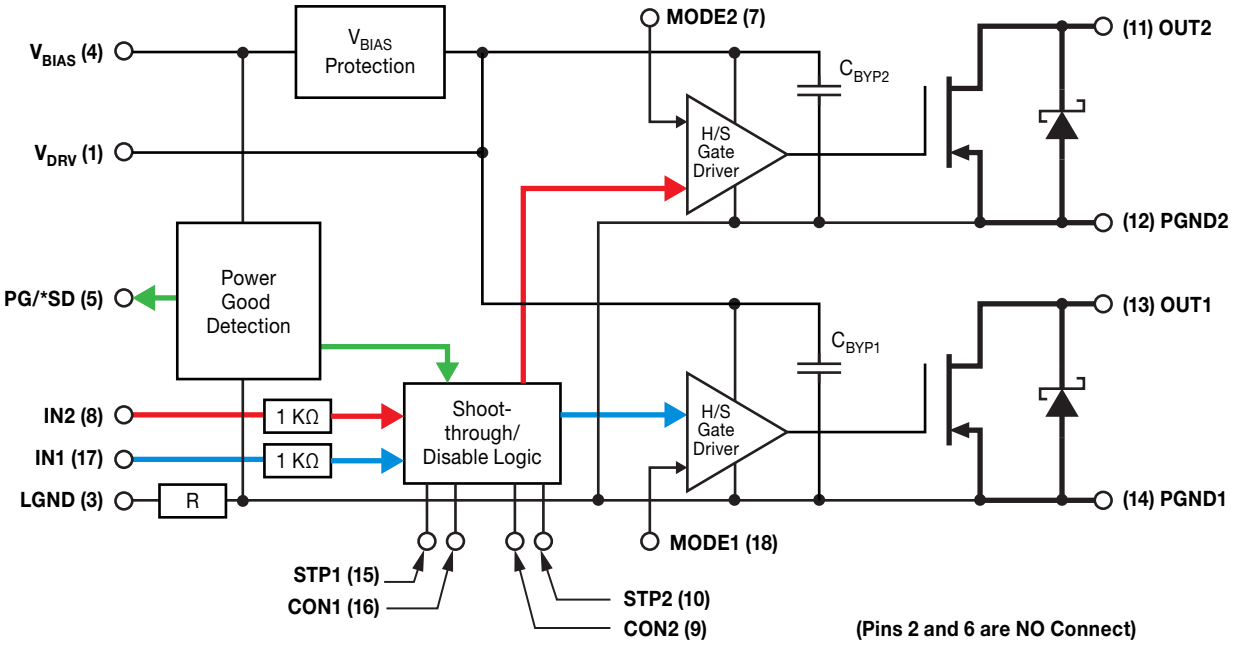
FBS-GAM04-P-C50

50 V_{DC}/10 A Dual Low-Side Power Driver Development Module

Description

EPC Space's "GaN Driving GaN Technology" **FBS-GAM04-P-C50** Series Dual Low-Side Power Driver Development Module incorporates eGaN® switching power HEMTs as two **output power switches**, two high speed **gate drive circuits** (consisting entirely of eGaN® switching elements), **input shoot-through protection** for circuits requiring such protection feature, **V_{BIAS} over-voltage clamp protection** and **+5 V_{DC} gate drive bias "power good" under-voltage monitoring circuitry** in an innovative, space-efficient, 18 pin SMT molded epoxy package provides for an excellent engineering brass-board development platform for the FBS-GAM04-P-R50 flight unit version.

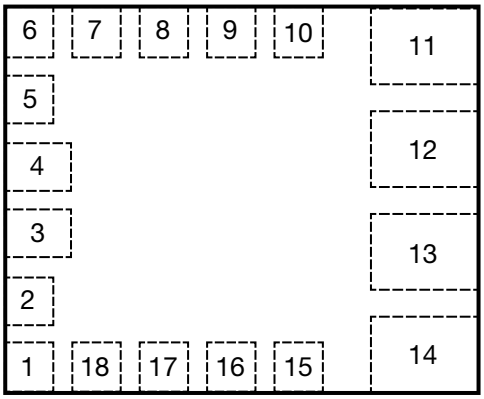
FBS-GAM04-P-C50 Functional Block Diagram



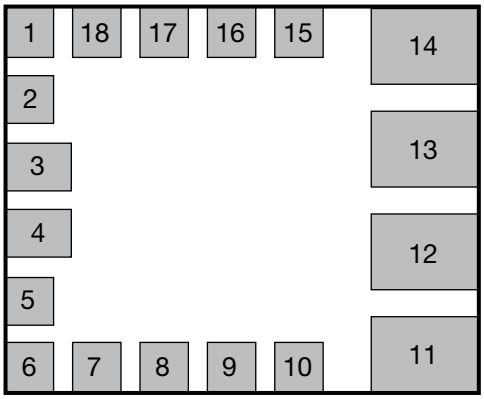
FBS-GAM04-P-C50 Functional Block Diagram

18 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



FBS-GAM04-P-C50 Configuration and Pin Assignment Table

Pin #	Pin Name	Input/Output	Pin Function
1	V_{DRV}	--	Protected Gate Driver Internal Power Supply Bias Voltage
2	N/C	--	No Internal Connection
3	LGND	--	Logic Ground, 0 V_{DC} (Low Current) (Note 12)
4	V_{BIAS}	I	+5 V_{DC} Gate Driver Power Supply Bias Input Voltage
5	PG/*SD	I/O	Power Good Output/Shutdown Input
6	N/C	--	No Internal Connection
7	MODE2	I	Power Driver 2 Synchronous/DC Mode Select
8	IN2	I	Power Switch 2 Logic Input
9	CON2	I	Power Driver 2 Input Shoot-Through Protection Control Input
10	STP2	O	Power Driver 2 Input Shoot-Through Protection Output
11	OUT2	O	Power Switch Open Drain Output 2 (High Current)
12	PGND2	--	Power Supply Return 2, 0 V_{DC} (High Current)
13	OUT1	O	Power Switch Open Drain Output 1 (High Current)
14	PGND1	--	Power Supply Return 1, 0 V_{DC} (High Current)
15	STP1	O	Power Driver 1 Input Shoot-Through Protection Output
16	CON1	I	Power Driver 1 Input Shoot-Through Protection Control Input
17	IN1	I	Power Switch 1 Logic Input
18	MODE1	I	Power Driver 1 Synchronous/DC Mode Select

IMPORTANT NOTE: Pin 14 (PGND1) **MUST** be connected to Pin 12 (PGND2) on the application PCB.

Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions		Value	Units
V_{DS}	Power Switch Drain to Source Voltage (Note 1)	Fully De-Rated	50	V
		Component Capability	100	
I_{D1}, I_{D2}	Continuous Drain Current, Each Power Driver		10	A
V_{BIAS}	Gate Driver Bias Supply Voltage	DC	-0.3 to 6.0	V
		50 ms	7.5	
B_{IN}, T_{IN}	IN1 or IN2 Input Voltage		-0.3 to 5.5	V
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-40 to +130	°C
T_c	Case Operating Temperature Range		-40 to +85	
T_{sol}	Peak Package Mounting Surface Temperature <= 90 Seconds		225	
ESD	ESD class level		1A	

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JC}$	Thermal Resistance Junction to Case, Either eGaN® Power Switch (Note 3)	8.5	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case, Either Clamp Schottky Diode (Note 3)	20	

OUT1 and OUT2 Power Switch Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
OUT1 and OUT2 Driver Off-State Leakage Current	I_L	V_{DS} = 25 V_{DC}, IN1 = IN2 = 0.8 V_{DC} (Note 1)	T_C = 25°C		10	125	µA
			T_C = 85°C		75	250	
		V_{DS} = 50 V_{DC}, IN1 = IN2 = 0.8 V_{DC} (Note 1)	T_C = 25°C	-	15	170	
			T_C = 85°C	-	100	505	
		V_{DS} = 100 V_{DC}, IN1 = IN2 = 0.8 V_{DC} (Note 1)	T_C = 25°C		75		
			T_C = 85°C		550		
OUT1 and OUT2 Output ON-State Resistance	$R_{DS(on)}$	IN1 = IN2 = 3 V_{DC} I_D = 10 A (Notes 1, 2)	T_C = 25°C		7	13.5	mΩ
			T_C = 85°C	-	10	17.0	
			T_C = -45°C		5.5	10	
OUT1 and OUT2 Output Source-Drain Clamping Voltage	V_{SD}	IN1 = IN2 = 3 V_{DC} I_D = 10 A (Notes 1, 2)	T_C = 25°C		0.85	0.95	V
			T_C = 85°C		0.78	0.88	
			T_C = -45°C		0.98	1.15	

IN1, IN2 Logic Input Static Electrical Characteristics *(-40°C≤ TC ≤ 85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
Low Logic Level Input Voltage	V_{IL}	V_{BIAS} = 5 V_{DC} (Note 4)				0.8	V
High Logic Level Input Voltage	V_{IH}	V_{BIAS} = 5 V_{DC} (Note 5)		2.9			
Low Logic Level Input Current	I_{IL}	V_{BIAS} = 5 V_{DC}, V_{IL} = 0.4 V	T_C = 25°C	-5	+/-1	5	µA
			T_C = 85°C	-30	+/-10	30	
High Logic Level Input Current	I_{IH}	V_{BIAS} = 5 V_{DC}, V_{IH} = 5 V	T_C = 25°C	-5	+/-1	5	
			T_C = 85°C	-30	+/-10	30	

V_{BIAS} Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} Recommended Operating Voltage Range	V_{BIAS}	(Note 3)	4.75		5.25	V
V_{BIAS} Operating Current	I_{BIAS}	V_{BIAS} = 5.25 V_{DC}		15	20	mA

PG Logic Output Static Electrical Characteristics *(-40°C≤ TC ≤ 85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Low Logic Level Output Voltage	V_{OL}	V_{BIAS} = 5 V_{DC} (Notes 6, 7)			0.2	V
High Logic Level Output Voltage	V_{OH}	V_{BIAS} = 5 V_{DC} (Notes 6, 7)	3.5			
Low Logic Level Output Sink Current	I_{OL}	V_{BIAS} = 5 V_{DC} (Note 8)			5	mA
High Logic Level Output Leakage Current	I_{OH}	V_{BIAS} = 5.25 V_{DC} (Note 8)		100		µA

PG Functional Static Electrical Characteristics *(-40°C≤ TC ≤ 85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} UVLO Rising Threshold	UVLO+	(Notes 6, 7, 8, 9)			4.7	V
V_{BIAS} UVLO Falling Threshold	UVLO-		2.95			
V_{BIAS} UVLO Hysteresis	UVLO+ - UVLO-			0.2		

OUT1 and OUT2 Power Switch Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
IN1-to-OUT1 or IN2-to-OUT2 Turn-ON Delay Time	$t_{d(on)}$	V_{DS} = 25 V_{DC}, I_D = 10 A (See Switching Figures)		26	34	ns
OUT1 or OUT2 Rise Time	t_r			10	14	
IIN1-to-OUT1 or IN2-to-OUT2 Turn-OFF Delay Time	$t_{d(off)}$			35	43	
OUT1 or OUT2 Fall Time	t_r			5	9	
OUT1-to-OUT2 Propagation Delay Skew	t_{d1-2}	(Note 10)		5		

Module Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Dynamic Gate/Driver Losses (Per Driver)	$P_{GD1, 2}$	V_{BIAS} = 5 V_{DC}		21		mW/MHz
Output Capacitance (Out-PGND)	$C_{OUT1, 2}$	V_{OUT} = 5 V_{DC}, f = 1 MHz		1020		pF
		V_{OUT} = 50 V_{DC}, f = 1 MHz		400		
Shoot-Through Protection Activation Delay Time	t_{st}	(Notes 3, 11)		5		ns
Schottky Output Diode ON-Time	t_{SD}	I_F = 10 A (Note 3)			100	
Minimum Switching Frequency	f_s	V_{DS} = 25 V_{DC}, I_D = 10 A (Note 3)	0			Hz
Maximum Switching Frequency				3		MHz

Specification Notes

1.) V_{BIAS} = +5 V_{DC}, PGND = LGND = 0 V_{DC} , V_{DS} = OUT1-to-PGND1 or V_{DS} = OUT2-to-PGND2 as specified.

2.) Measured using 4-Wire (Kelvin) sensing techniques.

3.) Guaranteed by design. Not tested in production.

4.) When either logic input (IN1 or IN2) is at the low input voltage level the associated output (OUT1 or OUT2) is guaranteed to be OFF (high impedance).

5.) When either logic input (IN1 or IN2) is at the high input voltage level the associated output (OUT1 or OUT2) is guaranteed to be ON (low impedance).

6.) Parameter measured with a 4.7 kΩ pull-up resistor between V_{DRV} and V_{BIAS}.

7.) PG is at a low level when V_{BIAS} is below the UVLO- (falling) threshold level or the OVLO+ (rising) threshold level. PG is at a high level when V_{BIAS} is above the UVLO+ (rising) threshold level or the OVLO- (falling) threshold level.

8.) PG is an open drain output referenced to LGND.

9.) V_{BIAS} levels below the UVLO- threshold result in both internal gate drivers being disabled: The logic inputs to the drivers are internally set to a logic low state to prevent damage to the eGaN® power switches.

10.) The OUT1-to-OUT2 propagation delay skew is defined as the time difference between the two outputs reaching either $t_{d(ON)}$ or $t_{d(OFF)}$ while being driven by the same input and driving an equivalent load.

11.) The input shoot-through protection is activated if both the IN1 and IN2 logic inputs are set to the logic high (“1”) condition simultaneously when pin 9 is connected to pin 10 and pin 15 is connected to pin 16.

12.) LGND to PGND1/PGND2 resistance is 1Ω typical.

Switching Figures

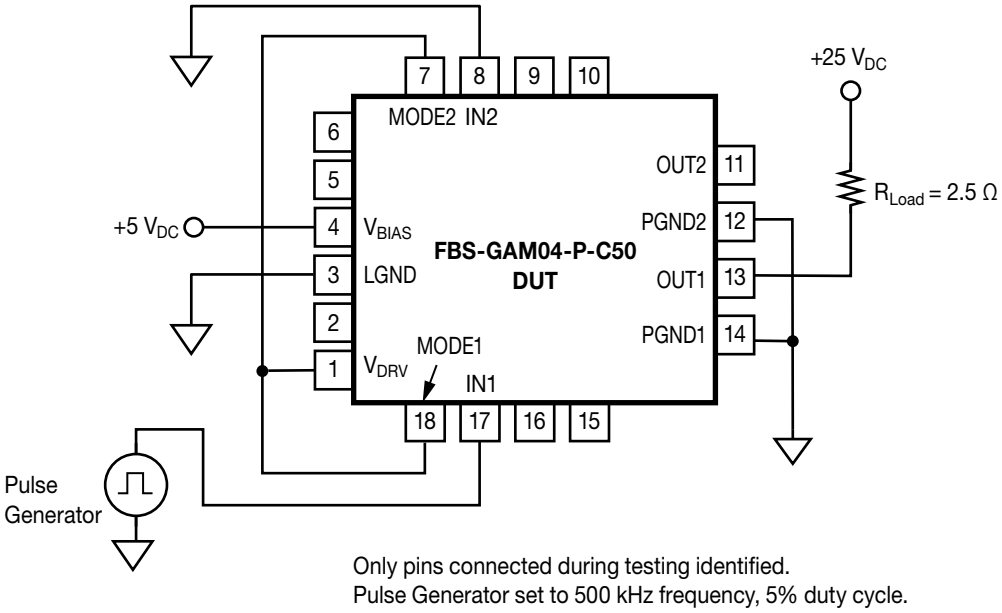
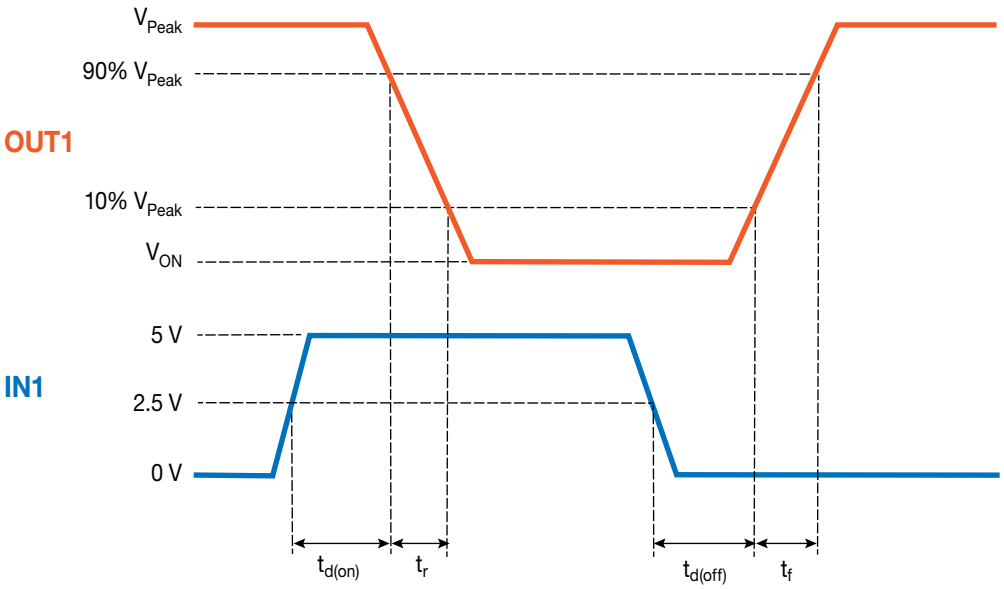


Figure 1. IN1-to-OUT1 Switching Time Test Circuit



NOTE: Waveforms exaggerated for clarity and observability.

Figure 2. IN1-to-OUT1 Switching Time Definition

Switching Figures *(continued)*

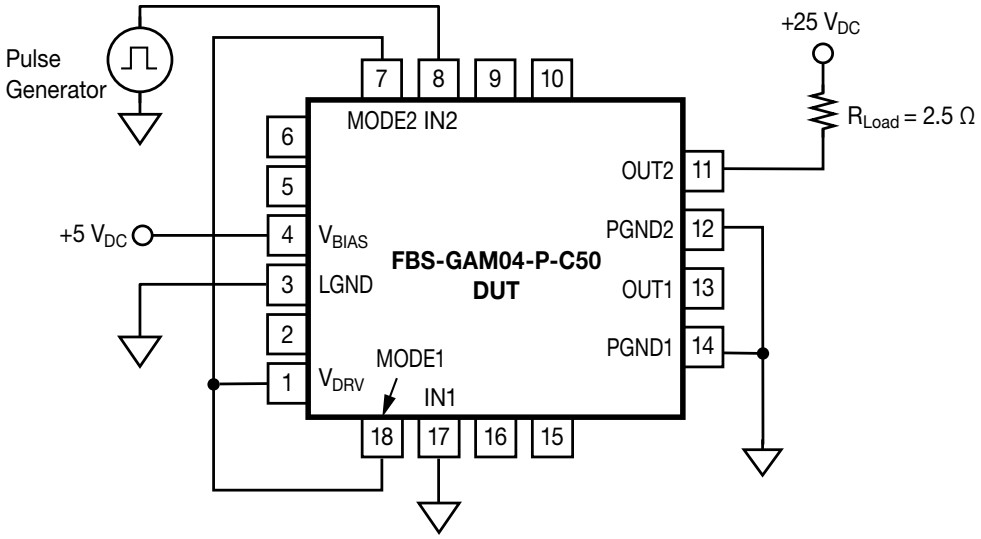
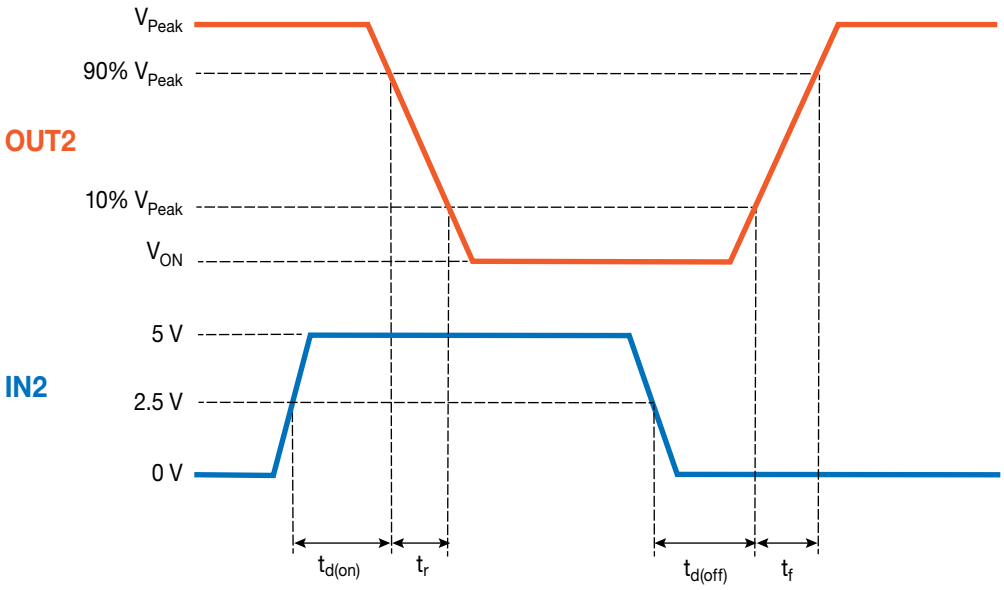


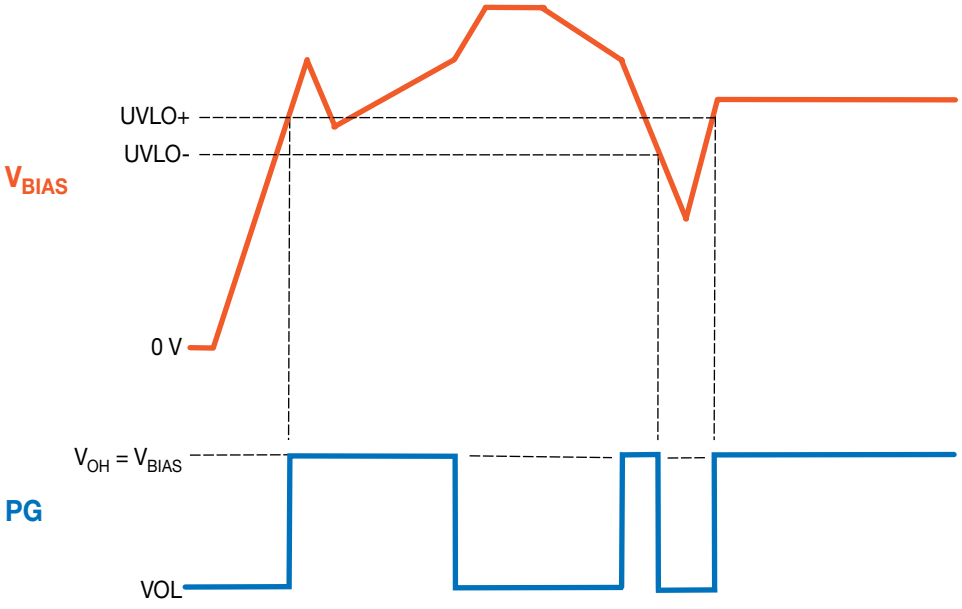
Figure 3. IN2-to-OUT2 Switching Time Test Circuit



NOTE: Waveforms exaggerated for clarity and observability.

Figure 4. IN2-to-OUT2 Switching Time Definition

Switching Figures *(continued)*



NOTE: Waveforms exaggerated for clarity and observability.

Figure 5. V_{BIAS}-to-PG Relationship

Typical Application Information

The following figures detail the suggested applications for the FBS-GAM04-P-C50 Module. For all applications, please refer to the following implementation sections, following, for proper power supply bypassing and layout recommendations and criteria. In any of the following applications, if an inductive load is driven then an appropriately-rated Schottky rectifier/diode should be connected across the load to prevent destructive flyback/"kickback" voltages from destroying the FBS-GAM04-P-C50.

In all the following figures, only the pins that are considered or that require connection are identified.

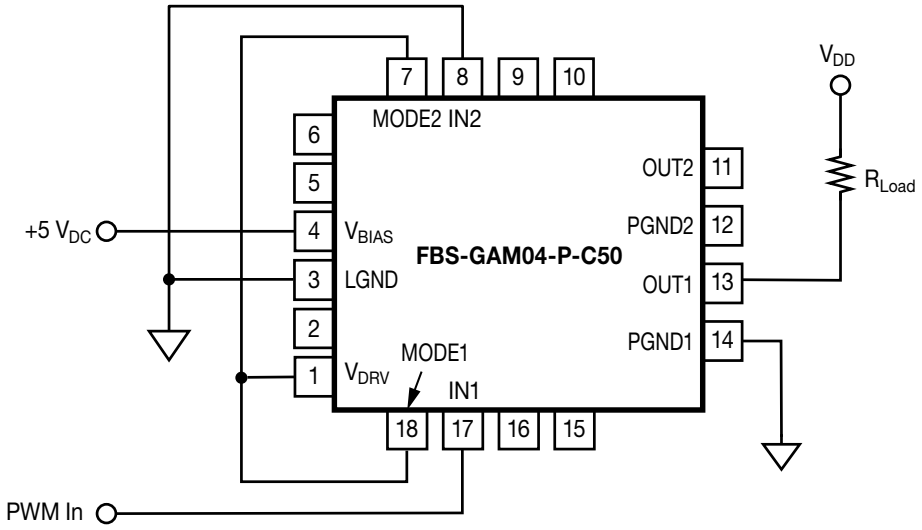


Figure 6. Single Low-Side Power Switch Configuration

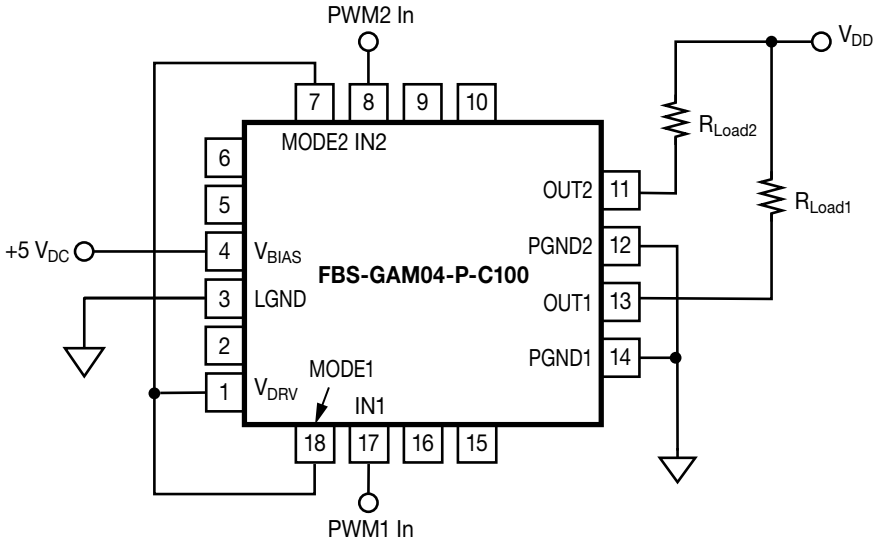


Figure 7. Dual Independent Low-Side Power Switches Configuration

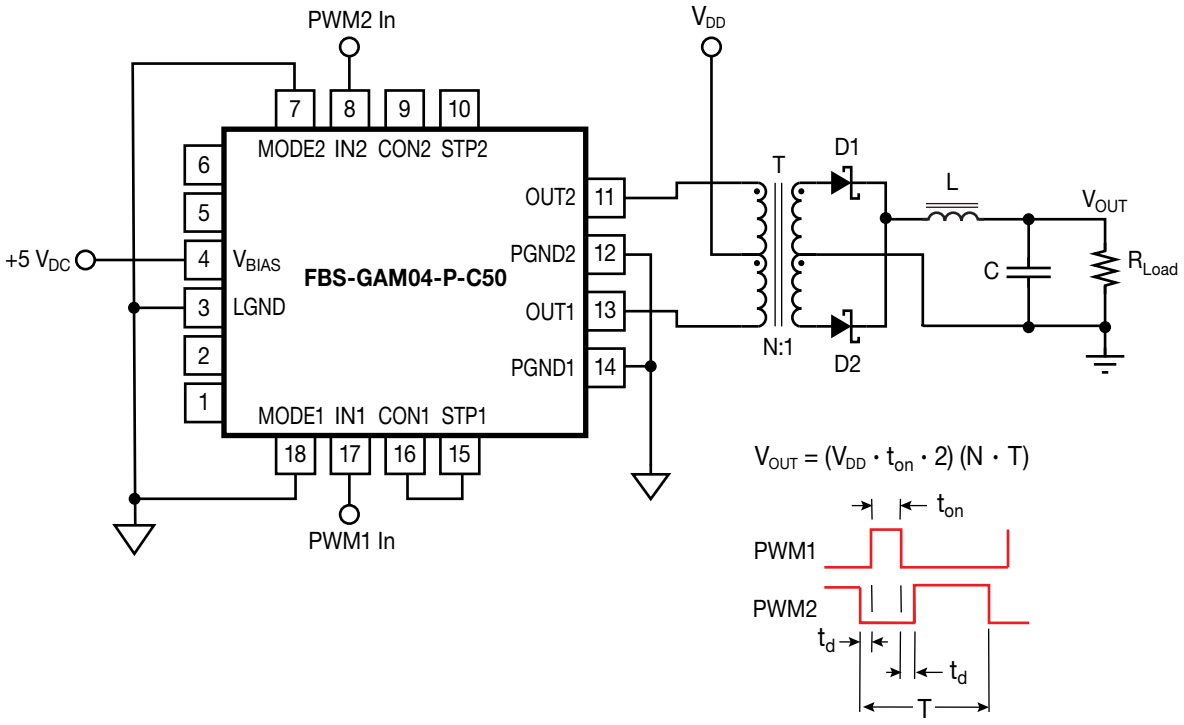


Figure 8. Dual Synchronous Switch Configuration: Push-Pull Converter

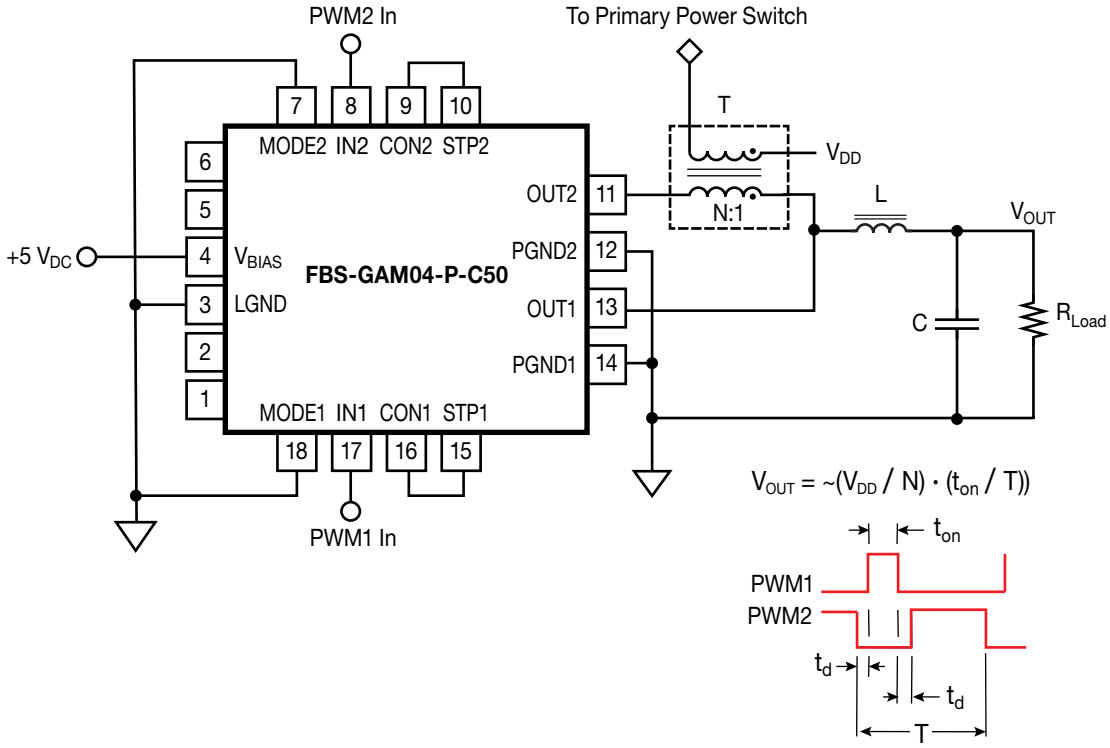


Figure 9. Dual Synchronous Switch Configuration: Synchronously-Rectified Forward Converter

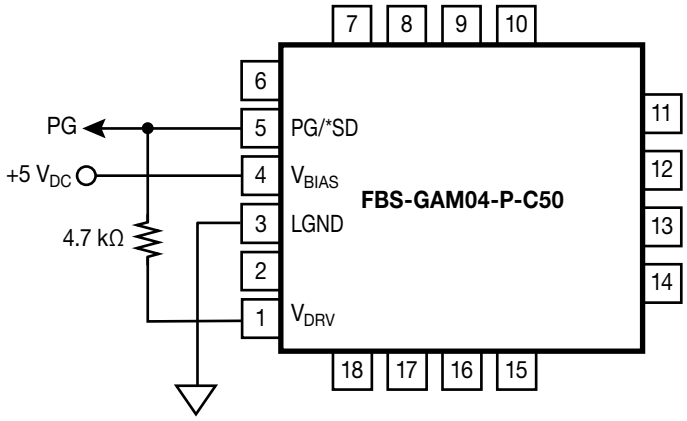


*Figure 10. PG/*SG Configured as PG (Power Good) Output*

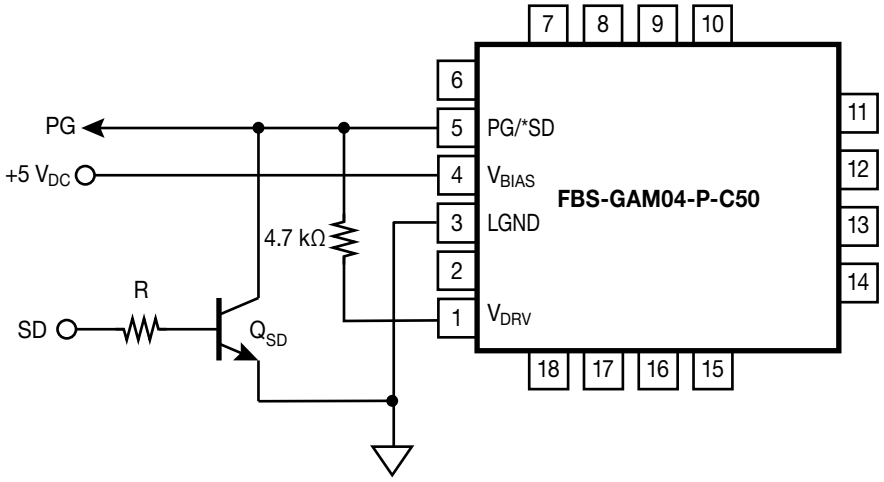


*Figure 11. PG/*SG Configured as *SD (Low-True Shutdown) Input*

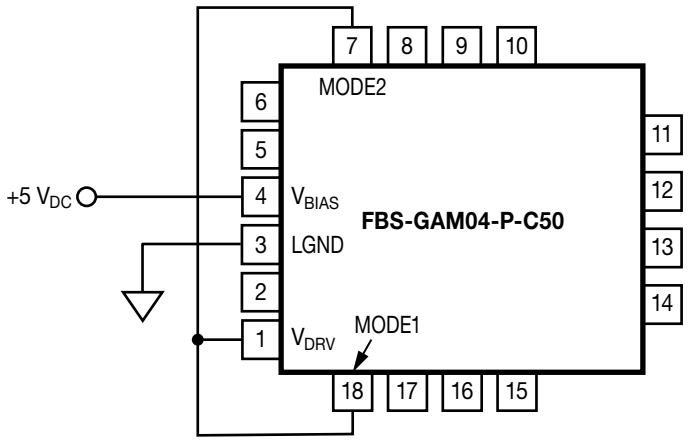


Figure 12. MODE Pin Selection Connection: DC Operation

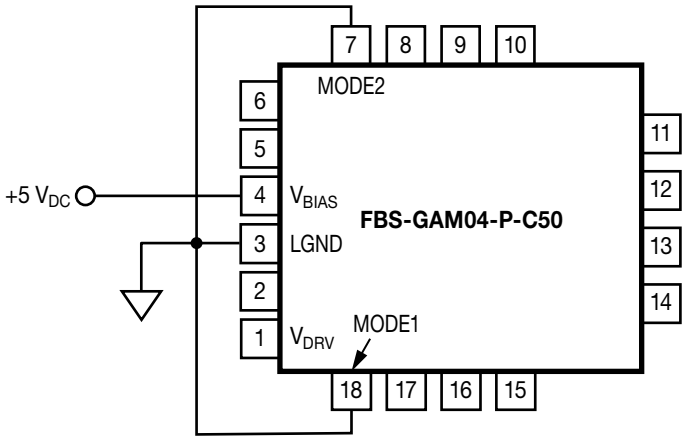
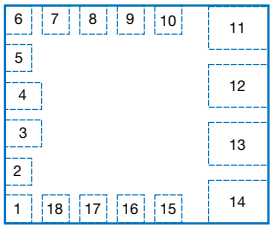


Figure 13. MODE Pin Selection Connection: Synchronous/Switching Operation

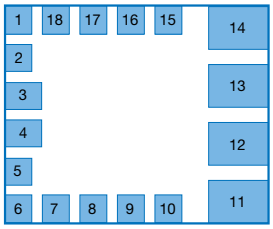
Pin Descriptions

18 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



V_{DRV} (Pin 1)

The V_{DRV} pin (Pin 1) of the FBS-GAM04-P-C50 is the protected V_{BIAS} power supply for the high-speed gate driver for the internal eGaN® power HEMT. This is a test pin for the module. This pin should be left OPEN (no connection) for proper operation of the module, unless otherwise directed in the "Typical Application Information" and "Pin Details" sections of this specification.

The FBS-GAM04-P-C50 incorporates circuitry for the internal gate drivers that clamps the voltage presented to the internal gate driver bias supply (+5 V_{DC} nominal) to a non-destructive maximum value. This prevents permanent damage from occurring to the gate drivers and the eGaN® power output HEMTs during voltage transient events greater than +6 V_{DC} that may occur during operation.

N/C (Pins 2 and 6)

Pins 2 and 186 are not internally connected. These "no connection" pins are recommended to be connected to the system PGND (ground plane) as good engineering practice to avoid coupling unwanted noise into the internal circuitry of the FBS-GAM04-P-C50.

LGND (Logic Ground) (Pin 3)

For proper operation of the FBS-GAM04-P-C50, the LGND pin (Pin 3) MUST be connected directly to the system logic ground return in the application circuit.

V_{BIAS} (Pin 4)

The V_{BIAS} pin is the raw input DC power input for the FBS-GAM04-P-C50 module. It is recommended that a 1.0 microfarad ceramic capacitor and a 0.1 microfarad ceramic capacitor, each 25 V rating, be connected between V_{BIAS} (pin 4) and system power ground plane (the common tie point of PGND1 and PGND2) to obtain the specified switching performance.

PG/*SD (Power Good Output) (Pin 5)

The bidirectional Power Good (PG) output and Shutdown (*SD) input pin. To externally disable the FBS-GAM04-P-C50, with the OUT1 and OUT2 pins forced to the high-impedance (OFF) state, the PG/*SD pin should be connected to logic ground, such as via an open-drain/collector. The module also incorporates a Power Good (PG) sensing circuit that disables the driver when the +5 V_{DC} gate drive bias potential (V_{BIAS}) falls below an under-voltage threshold range as specified in the Table "PG Functional Static Electrical Characteristics" (See Page 4). During the time when the V_{BIAS} potential is below the pre-set threshold, the PG output (Pin 5) pin is pulled low (to LGND) via an internal open drain. For proper module operation, when the V_{BIAS} potential is above the pre-set threshold the PG pin is pulled high via a 4.7 kΩ external pull-up resistor to V_{DRV} (pin 3).

MODE2 (Pin 7)

The MODE2 pin is the DC or synchronous/switching selection input for the FBS-GAM04-P-C50 module.

The MODE2 pin should be connected to PGND2 (pin 12) if synchronous/switching operation is desired. This connection prevents unwanted cross-conduction/shoot-through conditions from existing between the two drivers in the GAM04 during power V_{DD} and V_{BIAS} power sequencing. If DC operation or if independent operation of the two drivers in the GAM04 module is desired, the MODE2 pin should be connected to V_{DRV} (pin 1).

In NO case should the MODE2 pin be left open or connected to any other pin or potential.

IN2 (Pin 8)

The IN2 pin is the logic input for power driver 2. When the IN2 input pin is logic low ("0"), the OUT2 pin (pin 11) is in the low (low impedance) state. When the IN2 pin is logic high ("1"), the OUT2 pin is in the high (open) state.

CON2 (Pin 9)

The CON2 pin is the logic input for the input shoot-through protection for power driver 2. The state of this pin follows the state of the IN2 logic input pin. If input shoot-through protection is desired, for example in the case of a synchronously-rectified application (see Figure 9) where both power drivers (1 and 2) must not be turned on simultaneously, then CON2 (pin 9) should be externally connected to STP2 (pin 10). If no shoot-through protection is desired, then pin 9 should be left OPEN (no connection).

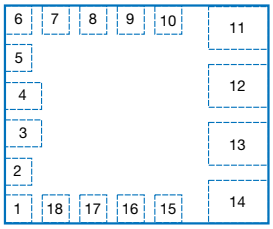
STP2 (Pin 10)

The STP2 pin is the open drain output for the input shoot-through protection for power driver 2. The state of this pin is the logical inverse of the IN1 logic input pin. If input shoot-through protection is desired, for example in the case of a synchronously-rectified application (see Figure 9) where both power drivers (1 and 2) must not be turned on simultaneously, then STP2 (pin 10) should be externally connected to CON2 (pin 9). If no shoot-through protection is desired, then pin 10 should be left OPEN (no connection).

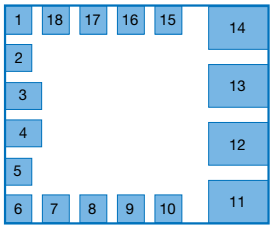
Pin Descriptions *(continued)*

18 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



OUT2 (Pin 11)

The OUT2 pin (pin 11) is the high current output (open drain) pin for the internal power eGaN® HEMT associated with power driver 2. This is a VERY high dV/dt and dI/dt pin and the connection to the external load should be as short as possible to minimize radiated EMI.

PGND2 (Pin 12)

The PGND2 pin (pin 12) is the ground return (source) connection for the internal power circuitry eGaN® HEMT and high-speed gate driver circuitry associated with power driver 2. This pin should be connected directly to the system power return/ground plane to minimize common source inductance, and the voltage transients associated with this inductance. If load current sensing is required, this should be accomplished via a current sense transformer in series with the drain of the power HEMT (pin 11). Although PGND1 and PGND2 are internally connected in the FBS-GAM04-P-C50 module, they MUST be externally connected on the end-use application PCB.

OUT1 (Pin 13)

The OUT1 pin (pin 13) is the high current output (open drain) pin for the internal power eGaN® HEMT associated with power driver 1. This is a VERY high dV/dt and dI/dt pin and the connection to the external load should be as short as possible to minimize radiated EMI.

PGND1 (Pin 14)

The PGND1 pin (pin 14) is the ground return (source) connection for the internal power circuitry eGaN HEMT and high-speed gate driver circuitry associated with power driver 1. This pin should be connected directly to the system power return/ground plane to minimize common source inductance, and the voltage transients associated with this inductance. If load current sensing is required, this should be accomplished via a current sense transformer in series with the drain of the power HEMT (pin 13). Although PGND1 and PGND2 are internally connected in the FBS-GAM04-P-C50 module, they MUST be externally connected on the end-use application PCB.

STP1 (Pin 15)

The STP1 pin is the open drain output for the input shoot-through protection for power driver 1. The state of this pin is the logical inverse of the IN2 logic input pin. If input shoot-through protection is desired, for example in the case of a synchronously-rectified application (see Figure 9) where both power drivers (1 and 2) must not be turned on simultaneously, then STP1 (pin 15) should be externally connected to CON1 (pin 16). If no shoot-through protection is desired, then pin 15 should be left OPEN (no connection).

CON1 (Pin 16)

The CON1 pin is the logic input for the input shoot-through protection for power driver 1. The state of this pin follows the state of the IN1 logic input pin. If input shoot-through protection is desired, for example in the case of a synchronously-rectified application (see Figure 9) where both power drivers (1 and 2) must not be turned on simultaneously, then CON1 (pin 16) should be externally connected to STP1 (pin 15). If no shoot-through protection is desired, then pin 16 should be left OPEN (no connection).

B_{STP} (Pin 16)

The B_{STP} pin is the open drain output for the input shoot-through protection for low-side gate driver. The state of this pin is the logical inverse of the T_{IN} logic input pin. If input shoot-through protection is desired, for example in the case of a half-bridge application (see Figure 9) where the low- and high-side gate drivers must not be turned on simultaneously, then B_{STP} (pin 16) should be externally connected to B_{CON} (pin 15). If no shoot-through protection is desired, then pin 16 should be left OPEN (no connection).

IN1 (Pin 17)

The IN1 pin is the logic input for power driver 1. When the IN1 input pin is logic low (“0”), the OUT1 pin (pin 13) is in the low (low impedance) state. When the IN1 pin is logic high (“1”), the OUT1 pin is in the high (open) state.

MODE1 (Pin 18)

The MODE1 pin is the DC or synchronous/switching selection input for the FBS-GAM04-P-C50 module.

The MODE1 pin should be connected to PGND1 (pin 14) if synchronous/switching operation is desired. This connection prevents unwanted cross-conduction/shoot-through conditions from existing between the two drivers in the GAM04 during power VDD and VBIAS power sequencing. If DC operation or if independent operation of the two drivers in the GAM04 module is desired, the MODE1 pin should be connected to VDRV (pin 1).

In NO case should the MODE1 pin be left open or connected to any other pin or potential.

Recommended V_{DD}-to-PGND Power Supply Bypassing

The V_{DD} power supply associated with the OUT high current output of the FBS-GAM04-P-C50 requires proper high frequency bypassing to PGND in-order to prevent harmful switching noise-related spikes from degrading or damaging the internal circuitry in the FBS-GAM04-P-C50 module, or impacting operating performance. It is recommended that a minimum of two (2) 4.7 microfarad ceramic capacitors, one (1) 1.0 microfarad ceramic capacitor and one (1) 0.1 microfarad ceramic capacitor, all with 100 V_{DC} ratings, be connected from V_{DD} to PGND. All four of these capacitors should be low ESR types, if possible. It is strongly recommended that these capacitors inscribe the smallest possible loop area between V_{DD} and PGND so-as to minimize the inductance, and thus voltage transients, related to this loop area. Regardless, different end-use implementations will require different V_{DD} bypass capacitor placements, and it is strongly recommended that the chosen bypassing scheme be evaluated for its effectiveness.

Recommended V_{BIAS}-to-PGND Power Supply Bypassing

It is also recommended that a 1.0 microfarad ceramic capacitor and a 0.1 microfarad ceramic capacitor, each 25 V_{DC} rating, be connected between V_{BIAS} (pin 4) and PGND (pin 14).

Input Shoot Through Protection

The FBS-GAM04-P-C50 is equipped with input shoot-through protection. This feature is activated whenever pins STP1 and CON1 are connected to each-other and STP2 and CON2 are connected to each-other. The input shoot through protection is a prevention mechanism to prevent the OUT1 and OUT2 power outputs from being activated simultaneously when the GAM04 Module is used in an application where it is prohibited that both switches be activated (turned “ON”) simultaneously, such as shown in Figures 8 and 9. If for some unforeseen reason the PWM controller at the IN1 and IN2 logic inputs presented simultaneous logic 1 (high) signals to the GAM04 Module, the OUT1 and OUT2 power outputs would each revert to their open (OFF) state, thus preventing a simultaneous ON condition.

CAUTION: *The input shoot through protection does not guarantee output shoot-through protection during normal PWM switching operation*. Output shoot-through protection is implemented by the end-user in the form of the proper logic input signal delays to ensure that the OUT1 and OUT2 power outputs are never simultaneously ON dynamically or in the steady state. Thus, it is incumbent upon the end user to add the proper delay or “dead” times at each switching state change of the IN1 and IN2 logic inputs to account for the ON- and OFF-delay times for each driver. A dead time of 75 ns, minimum, between the fall of the IN1 logic input and the rise of the IN2 logic input or between the fall of the IN2 logic input and the rise of the IN1 logic input is adequate to prevent shoot-through between the OUT1 and OUT2 power outputs.

DC Operation and Synchronous /Switching Operation

Each driver in the FBS-GAM04 is equipped with a mode select pin (MODE1 or MODE2). These pins allow each driver to be configured as a DC switch, as a high frequency switch or as a synchronous pair (such as in the output stage of a synchronously-rectified forward converter, see Figure 9). When DC operation is desired/required, the MODE pin(s) should be tied to V_{DRV} pin to ensure that steady-state bias is provided to the gate driver(s). When synchronous (complementary) or switching operation is desired/required, then the MODE pin(s) should be tied to the corresponding PGND for the driver (1 or 2). This connection insures that during power-on or power-off events that the two drivers cannot turn ON simultaneously during the VBIAS power supply ramp-up or ramp-down.

Calculating FBS-GAM04 Module Power Losses and Efficiencies

The driver power losses for the FBS-GAM04 Module are determined as follows:

$$P_D(\text{Driver}) = P_{Gate}(DC) + P_{Gate}(AC) + P_{Switch}(DC) + P_{Switch}(\text{Switching}) + P_{Switch}(C_{OUT}),$$
$$\text{and } P_D(\text{Schottky}) = P_{\text{dead time}},$$

where $P_{Gate}(DC)$ are the DC gate/gate driver losses ($V_{BIAS} \cdot I_{BIAS} \cdot 0.5$), $P_{Gate}(AC)$ are the dynamic gate/gate driver losses ($P_{GD} \cdot f_s$), $P_{Switch}(DC)$ are the power switch DC losses ($I_D^2 \cdot R_{DS(on)} \cdot ton / T$), $P_{Switch}(\text{Switching})$ are the power switch losses related to the switching event [$(0.5 \cdot V_{DD} \cdot I_D \cdot tr / T) + (0.5 \cdot V_{DD} \cdot I_D \cdot t_f / T)$], $P_{Switch}(C_{OUT})$ are the losses related to switching the total drain capacitance C_{OUT} ($0.5 \cdot C_{OUT} \cdot V_{DD}^2 \cdot f_s$), and P_{dead} time are the losses related to the Schottky catch diode conduction time, which occurs during the delay "dead" time between driver switching events ($2 \cdot V_{SD} \cdot I_D \cdot t_{SD} / T$) as there are two driver switching events per period. The quantities I_{BIAS}, P_{GD}, $R_{DS(on)}$, t_r, t_f, C_{OUT} and V_{SD} may be found in the parametric tables found on pages 4 and 5, and the quantities V_{DD}, V_{BIAS}, f_s, t_{on} (the ON time of the power switch), T ($1 / f_s$) and t_{SD} are determined by the conditions of operation of the FBS-GAM04-P-R100 module.

For example, if the GAM04 drivers are operated in a synchronous rectifier application (see Figure 4), one driver will have an on time of ton and the other will have an on time of ($T - t_{on}$), and if the duty cycle is set to 50%, the power losses for the two drivers will be approximately equal. The following example calculates the losses for each driver empirically:

$$V_{DD} = 25\ V_{DC},\ I_D = 10\ A,\ V_{BIAS} = 5\ V_{DC},$$
$$f_s = 750\ kHz,\ T = 1/f_s = 1.33\ \mu s,\ t_{on} = 0.333\ \mu s\ (25\%\ \text{duty cycle}),\ t_{SD} = 40\ ns \text{ and } T_A = 25°C.$$

The associated losses for Driver 1 and Driver 2 are shown in the following two tables:

Table I. Driver 1 Power Loss Tabulation

Driver 1 (operating at t_{on})			
Loss	**Equation**	**Equation w/Values**	**Result**
$P_{Gate}(DC)$	$V_{BIAS} \cdot I_{BIAS} \cdot 0.5$	$5 \cdot 0.017 \cdot 0.5$	0.04 W
$P_{Gate}(AC)$	$P_{GD} \cdot f_s$	$0.021 \cdot 0.75^{(1)}$	0.02 W
$P_{Switch}(DC)$	$I_D^2 \cdot R_{DS(on)} \cdot t_{on} / T$	$10^2 \cdot 0.01 \cdot 0.33/1.33$	0.25 W
$P_{Switch}(\text{Switching})$	$(0.5 \cdot V_{DD} \cdot I_D \cdot t_r / T) +$ $(0.5 * V_{DD} \cdot I_D \cdot t_f / T)$	$(0.5 \cdot 25 \cdot 10 \cdot 0.008/1.33) +$ $(0.5 \cdot 25 \cdot 10 \cdot 0.010/1.33)$	1.69 W
$P_{Switch}(C_{OUT})$	$0.5 \cdot C_{OUT} \cdot V_{DD}^2 \cdot f_s$	$0.5 \cdot 1150 \cdot 10^{-12} \cdot 25^2 \cdot 750000$	0.27 W
$P_D(\text{Schottky})$	$2 \cdot V_{SD} \cdot I_D \cdot t_{SD} / T$	$2 \cdot 0.95 \cdot 10 \cdot 0.04/1.33$	0.57 W
P1 Total			**2.84 W**

Note: (1) 750 kHz is 0.75 MHz

Table II. Driver 2 Power Loss Tabulation

Driver 2 (operating at T - t_{on})			
Loss	**Equation**	**Equation w/Values**	**Result**
P_{Gate}(DC)	$V_{BIAS} \cdot I_{BIAS} \cdot 0.5$	$5 \cdot 0.017 \cdot 0.5$	0.04 W
P_{Gate}(AC)	$P_{GD} \cdot f_s$	$0.021 \cdot 0.75^{(1)}$	0.02 W
P_{Switch}(DC)	$I_D^2 \cdot R_{DS(on)} \cdot t_{on} / T$	$10^2 \cdot 0.01 \cdot 0.66/1.33$	0.50 W
P_{Switch}(Switching)	$(0.5 \cdot V_{DD} \cdot I_D \cdot t_r / T) +$ $(0.5 * V_{DD} \cdot I_D \cdot t_f / T)$	$(0.5 \cdot 25 \cdot 10 \cdot 0.008/1.33) +$ $(0.5 \cdot 25 \cdot 10 \cdot 0.010/1.33)$	1.69 W
$P_{Switch}(C_{OUT})$	$0.5 \cdot C_{OUT} \cdot V_{DD}^2 \cdot f_s$	$0.5 \cdot 1150 \cdot 10^{-12} \cdot 25^2 \cdot 750000$	0.27 W
P_D(Schottky)	$2 \cdot V_{SD} \cdot I_D \cdot t_{SD} / T$	$2 \cdot 0.95 \cdot 10 \cdot 0.04/1.33$	0.57 W
P2 Total			**3.09 W**

Note: (1) 750 kHz is 0.75 MHz

The total GAM04 module loss is P1(TOTAL) + P2(TOTAL) = 2.84 + 3.09 = 5.93 W. The power delivered to the load is $V_{DD} \cdot I_D \cdot t_{on} / T$, or 62.5 W. The conversion efficiency for the GAM04 module, η, is $P_{LOAD} / (P_{LOAD} + P_{LOSS})$ = 62.5 / 68.4 = 91.4%.

It is clear in the previous power loss/efficiency example that the majority of the losses experienced by the GAM04 are related to dynamic losses. Thus, to achieve the lowest losses and highest possible efficiency, it is desirable to operate the synchronously- rectified circuit with the lowest possible V_{DD} potential. For example, if the V_{DD} potential in the previous example is reduced from 25 V_{DC} to 12 V_{DC} (e.g. changing the primary-to-secondary winding ratio of the power transformer), the total module losses are reduced from 5.93 W to 4.00 W, a nearly 2.0 W reduction – and the conversion efficiency increases to 94%. This might be a design tradeoff (transformer design versus an increased efficiency of approximately 2.2%) worthy of consideration if the transformer re-design does not incur additional power losses.

Suggested FBS-GAM04-P-C50 Schematic Symbol

The suggested schematic symbol for the FBS-GAM04-P-C50 is shown in Figure 6. This symbol groups the I/O pins of the FBS-GAM04-P-C50 into groups of similar functionality.

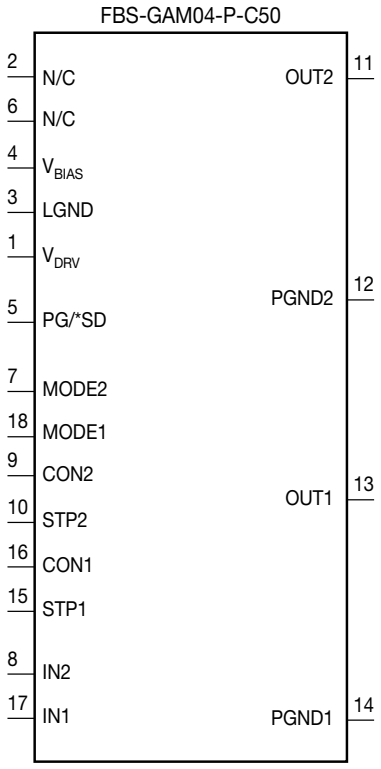


Figure 14. Suggested FBS-GAM04-P-C50 Schematic Symbol

Thermal Characteristics

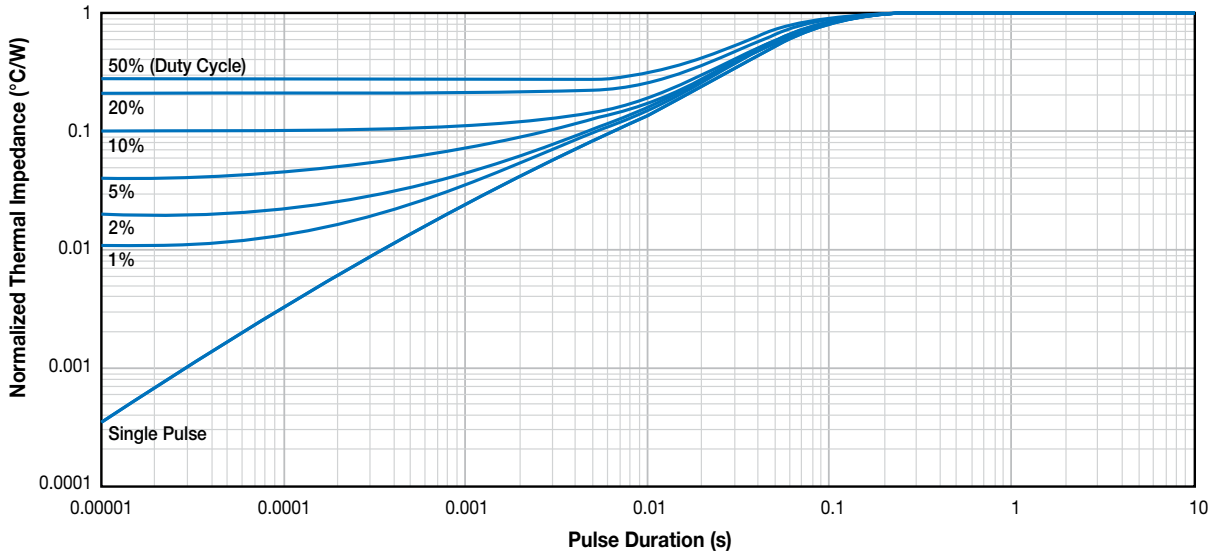


Figure 15. Typical Power eGAN® HEMT Normalized Junction-to-Case Thermal Impedance

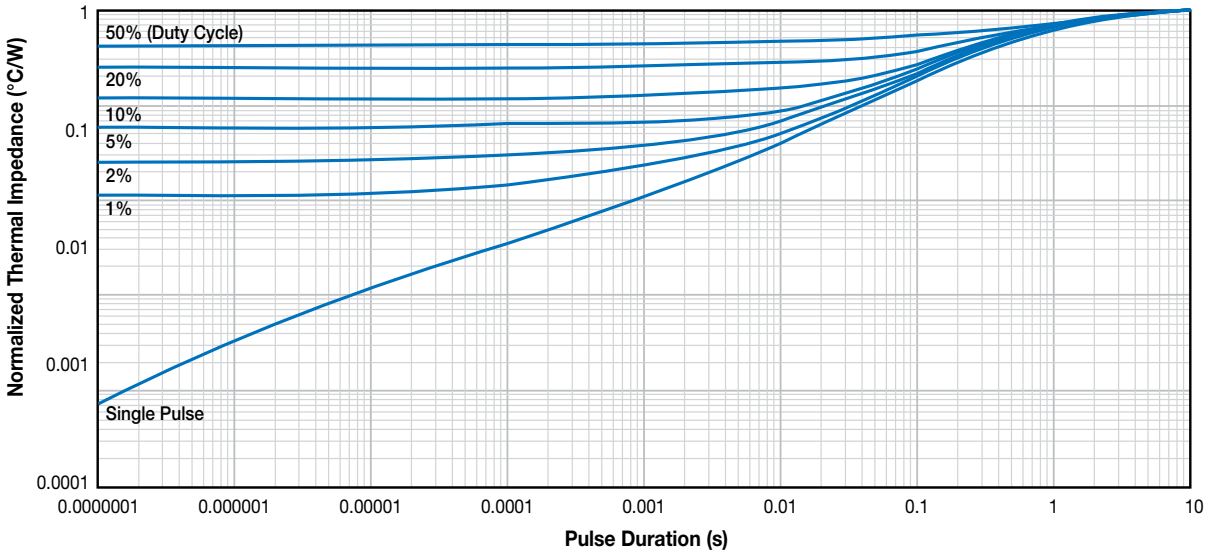
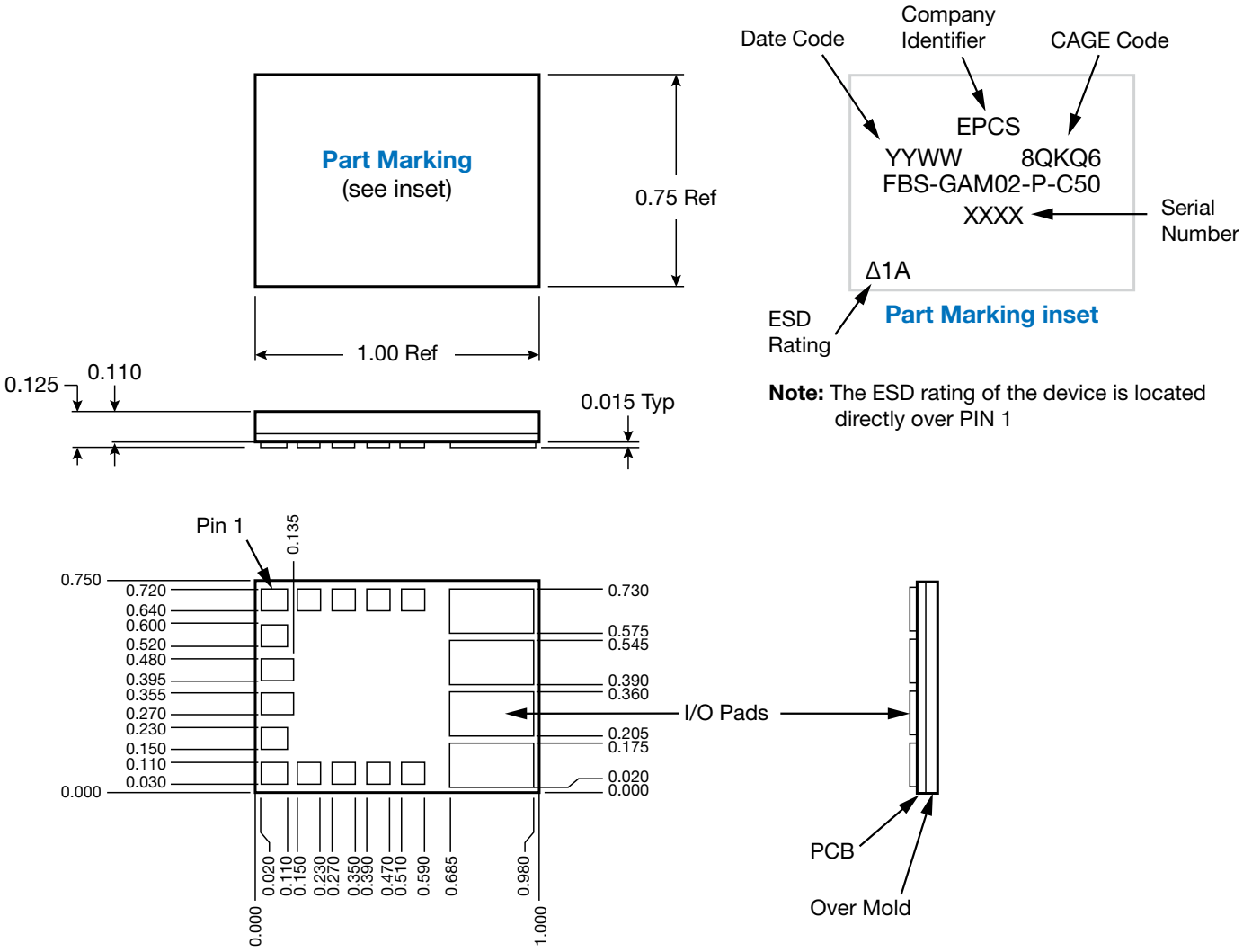


Figure 16. Typical Catch Schottky Normalized Junction-to-Case Thermal Impedance

Package Outline, Dimensions, and Part Marking



Note: All dimensions are in inches
ALL tolerances +/- 0.010

Figure 17. FBS-GAM04-P-C50 Package Outline and Dimensions

Recommended PCB Solder Pad Configuration

The novel I/O "pillar" pads fabricated onto the bottom surface of the FBS-GAM04-P-C50 module are designed to provide optimal electrical, thermal and mechanical properties for the end-use system designer. To achieve the full benefit of these properties, it is important that the FBS-GAM04-P-C50 module be soldered to the PCB motherboard using SN63 (or equivalent) solder. Care should be taken during processing to insure there is minimal solder voiding in the contacts to the OUT2 (pin 11), PGND1 (pin 12), OUT1 (pin 13) and PGND2 (Pin 14) pads on the module. The recommended pad dimensions and locations are shown in Figure 17. All dimensions are shown in inches.

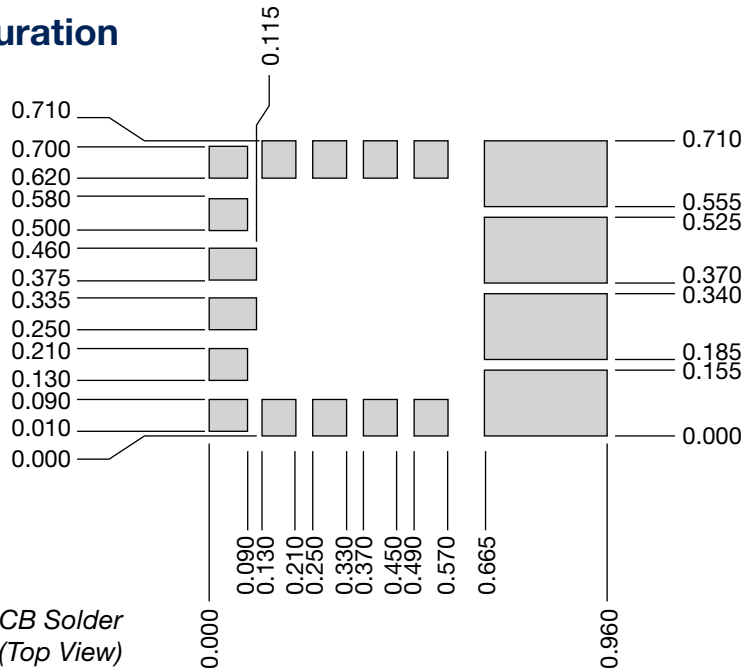


Figure 18. Recommended PCB Solder Pad Configuration (Top View)

Sn63/Pb37 No Clean Solder Paste Typical Example Profile

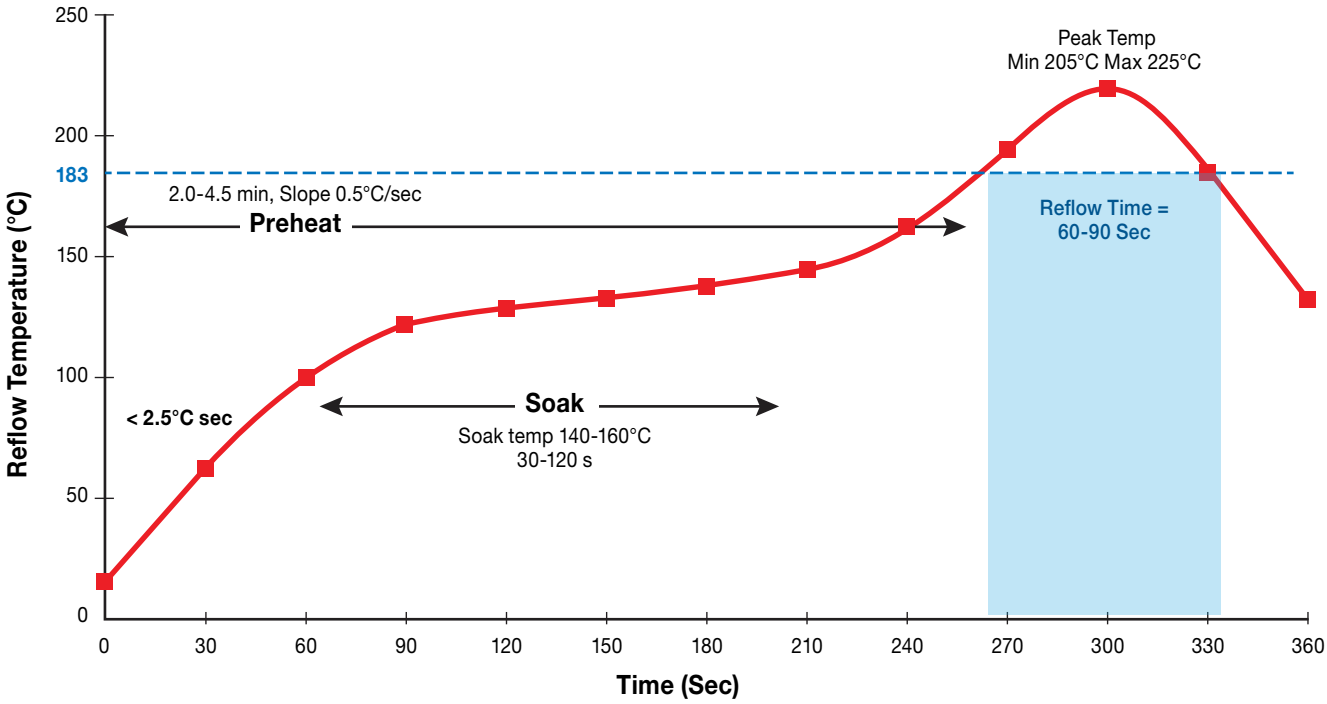


Figure 19. Typical GAM02P-PSE Solder Reflow Profile

Preheat Zone – The preheat zone, is also referred to as the ramp zone, and is used to elevate the temperature of the PCB to the desired soak temperature. In the preheat zone the temperature of the PCB is constantly rising, at a rate that should not exceed 2.5°C/sec. The oven's preheat zone should normally occupy 25-33% of the total heated tunnel length.

The Soak Zone – normally occupies 33-50% of the total heated tunnel length exposes the PCB to a relatively steady temperature that will allow the components of different mass to be uniform in temperature. The soak zone also allows the flux to concentrate and the volatiles to escape from the paste.

The Reflow Zone – or spike zone is to elevate the temperature of the PCB assembly from the activation temperature to the recommended peak temperature. The activation temperature is always somewhat below the melting point of the alloy, while the peak temperature is always above the melting point.

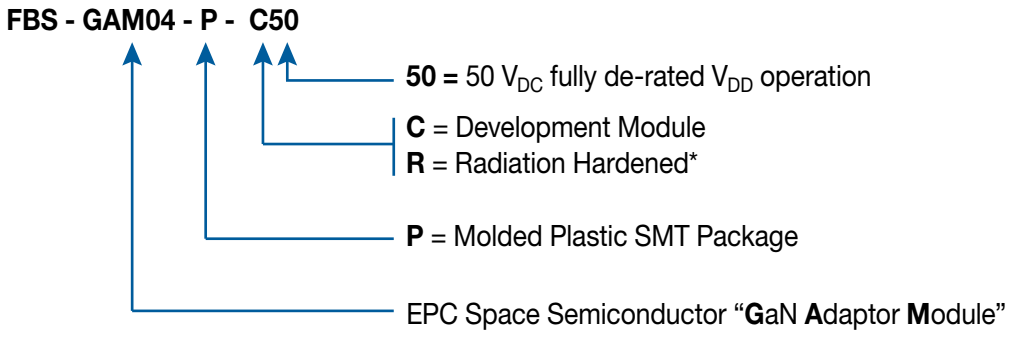
Reflow – Best results achieved when reflowed in a ***forced air convection*** oven with a minimum of 8 zones (top & bottom), however reflow is possible with a four-zone oven (top & bottom) with the recommended profile for a forced air convection reflow process. The melting temperature of the solder, the heat resistance of the components, and the characteristics of the PCB (i.e. density, thickness, etc.) determine the actual reflow profile.

Note: FBS-GAM04-P-C50 solder attachment has a maximum peak dwell temperature of 225°C limit, exceeding the maximum peak temperature can cause damage the unit.

Reflow Process Disclaimer

The profile is as stated "Example". The-end user can optimize reflow profiling based against the actual solder paste and reflow oven used. EPC Space assumes no liability in conjunction with the use of this profile information.

EPC Space Part Number Information



*FBS-GAM04-P-C50 (Utilizes High Lead Content Die)

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Revisions

Datasheet Revision	Product Status
REV -	Proposal/development
M-702-012-Q1	Characterization and Qualification
	Production Released

Information subject to change without notice.
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