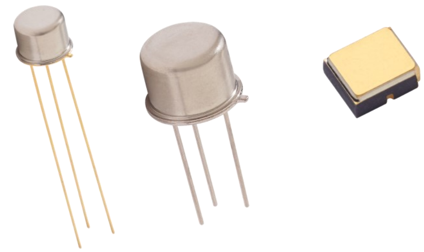
2N3498, 2N3499, 2N3500, 2N3501

NPN Medium Power Silicon Transistor

Rev. V3



Features

- Available in JAN, JANTX, JANTXV and JANS per MIL-PRF-19500/366
- TO-39 (TO-205AD) and TO-5 Leaded Packages
- 2N3501 Available In UB package
- Ideal for High Voltage Inductive Load Switching Applications

Electrical Characteristics (T_A = +25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Breakdown Voltage	I_C = 10 mA dc 2N3498, 2N3499 2N3500, 2N3501, 2N3501UB	$V_{(BR)CEO}$	V dc	100 150	—
Collector - Base Cutoff Current	V_{CB} = 100 V dc 2N3498, 2N3499 V_{CB} = 150 V dc 2N3500, 2N3501 2N3501UB	I_{CBO1}	µA dc	—	10
Collector - Base Cutoff Current	V_{CB} = 50 V dc 2N3498, 2N3499 V_{CB} = 75 V dc 2N3500, 2N3501 2N3501UB	I_{CBO2}	nA dc	—	50
Emitter - Base Cutoff Current	V_{EB} = 6.0 V dc	I_{EBO1}	µA dc	—	10
Emitter - Base Cutoff Current	V_{EB} = 4.0 V dc	I_{EBO2}	nA dc	—	25
Collector - Emitter Saturation Voltage	I_C = 10 mA dc; I_B = 1 mA dc	$V_{CE(SAT)1}$	V dc	—	0.2
Collector - Emitter Saturation Voltage	I_C = 150 mA dc; I_B = 15 mA dc (2N3500, 2N3501, 2N3501B only)	$V_{CE(SAT)2}$	V dc	—	0.4
Collector - Emitter Saturation Voltage	I_C = 300 mA dc; I_B = 30 mA dc (2N3498, 2N3499 only)	$V_{CE(SAT)3}$	V dc	—	0.6
Base - Emitter Saturation Voltage	I_C = 10 mA dc; I_B = 1 mA dc	$V_{BE(SAT)1}$	V dc	—	0.8
Base - Emitter Saturation Voltage	I_C = 150 mA dc; I_B = 15 mA dc (2N3500, 2N3501, 2N3501B only)	$V_{BE(SAT)2}$	V dc	—	1.2
Base - Emitter Saturation Voltage	I_C = 300 mA dc; I_B = 30 mA dc (2N3498, 2N3499 only)	$V_{BE(SAT)3}$	V dc	—	1.4
Collector - Base Cutoff Current	T_A = +150°C V_{CB} = 50 V dc 2N3498, 2N3499 V_{CB} = 75 V dc 2N3500, 2N3501 2N3501UB	I_{CBO3}	µA dc	—	50
Forward Current Transfer Ratio	T_A = -55°C V_{CE} = 10 V dc; I_C = 150 mA dc 2N3498, 2N3500 2N3499, 2N3501, 2N3501UB	h_{FE7}	-	22 45	

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info@vptcomponents.com

Electrical Characteristics (T_A = +25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 0.1 mA dc 2N3498, 2N3500 2N3499, 2N3501,2N3501 UB	h_{FE1}	-	20 35	
Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 1.0 mA dc 2N3498, 2N3500 2N3499, 2N3501,2N3501 UB	h_{FE2}	-	25 50	
Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 10 mA dc 2N3498, 2N3500 2N3499, 2N3501,2N3501 UB	h_{FE3}	-	35 75	
Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 150 mA dc 2N3498, 2N3500 2N3499, 2N3501,2N3501 UB	h_{FE4}	-	40 100	120 300
Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 300 mA dc 2N3500 2N3501, 2N3501 UB	h_{FE5}	-	15 20	
Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 500 mA dc 2N3498 2N3499	h_{FE6}	-	15 20	

Dynamic Characteristics					
Magnitude of Small-Signal Short-Circuit Forward Current Transfer Ratio	I_C = 20 mA dc; V_{CE} = 20 V dc; f = 100 mHz	$\|h_{fe}\|$	-	1.5	8
Small-Signal Short-Circuit Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_C = 10 mA dc; f = 1 kHz 2N3498, 2N3500 2N3499, 2N3501, 2N3501UB	h_{fe}		35 75	300 375
Open Circuit Output Capacitance	V_{CB} = 10 V dc; I_E = 0; 100 kHz $\leq f \leq$ 1 MHz 2N3489,2N3499 2N3500, 2N3501	C_{obo}	pF	—	10 8
Input Capacitance (Output Open Circuited)	V_{EB} = 0.5 V dc; I_C = 0; 100 kHz $\leq f \leq$ 1 MHz	C_{ibo}	pF		80
Switching Characteristics					
Turn-On Time	I_C = 150 mA dc; I_{B1} = 15 mA dc; V_{EB} = 5 V dc	t_{on}	ns	—	115
Turn-Off Time	I_C = 150 mA dc; I_{B1} = I_{B2} = 15 mA dc	t_{off}	ns	—	1150

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Absolute Maximum Ratings

Ratings	Symbol	Value
Collector - Emitter Voltage 2N3498 2N3499, L, U4 2N3500 2N3501, L, U4, UB	V_{CEO}	 100 V dc 150 V dc
Collector - Base Voltage 2N3498 2N3499, L, U4 2N3500 2N3501, L, U4, UB	V_{CBO}	 100 V dc 150 V dc
Emitter - Base Voltage	V_{EBO}	6.0 V dc
Collector Current 2N3498 2N3499, L, U4 2N3500 2N3501, L, U4, UB	I_C	 500 mA dc 300 mA dc
Total Power Dissipation @ T_A = +25°C[2] @ T_C = +25°C[3]	P_T	 1.0 W 6.0 W
Operating & Storage Temperature Range	T_{OP}, T_{STG}	-65°C to +200°C

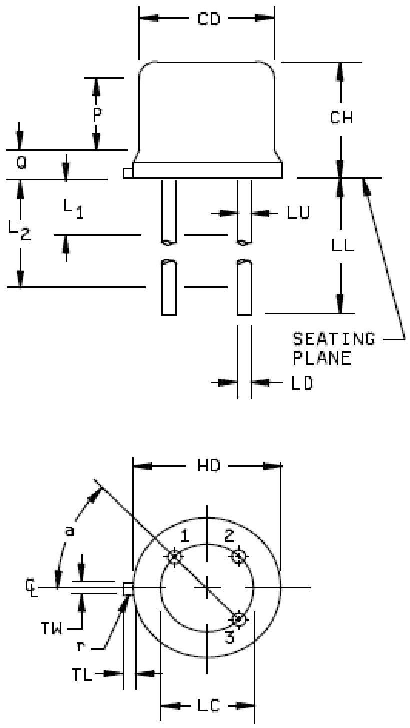
Thermal Characteristics

Types	P_T T_A= +25°C (1)	P_T T_C= +25°C (1)	P_T T_{SP}= +25°C (1)	$R_{\theta JA}$	$R_{\theta JC}$	$R_{\theta JC}$ Kovar	$R_{\theta JSP}$	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_J and T_{STG} -65 to +200
	W	W	W	°C/W	°C/W	°C/W	°C/W	V dc	V dc	V dc	mA dc	°C
2N3498,L	1	5	N/A	175	30	34.9	N/A	100	100	6	500	
2N3498U4	1	4	N/A	175	15		N/A	100	100	6	500	
2N3499,L	1	5	N/A	175	30	34.9	N/A	100	100	6	500	
2N3499U4	1	4	N/A	175	15		N/A	100	100	6	500	
2N3500,L	1	5	N/A	175	30	34.9	N/A	150	150	6	300	
2N3500U4	1	4	N/A	175	15		N/A	150	150	6	300	
2N3501,L	1	5	N/A	175	30	34.9	N/A	150	150	6	500	
2N3501U4	1	4	N/A	175	15		N/A	150	150	6	300	
2N3501UB	1	.5	1.5	350	N/A		90	150	150	6	300	

(1) Derating curves 6, 7, 8, 9 and 10 per MIL-PRF-19500/366

Safe Operating Area		
DC Tests:	T_C = +25°C; I Cycle; tr ≥ 10 ns; t =1s	
Test 1:	V_{CE} = 10 V dc; I_C = 500 mA dc	2N3498, 2N3499
	V_{CE} = 16.67 V dc; I_C = 300 mA dc	2N3500, 2N3501
	V_{CE} = 10 V dc; I_C = 113mA dc	2N3501UB
Test 2:	V_{CE} = 50 V dc; I_C = 100 mA dc	2N3498, 2N3499, 2N3500, 2N3501
	V_{CE} = 50 V dc; I_C = 23 mA dc	2N3501UB
Test 3:	V_{CE} = 80 V dc; I_C = 40 mA dc	2N3498, 2N3499, 2N3500, 2N3501
	V_{CE} = 80 V dc; I_C = 14 mA dc	2N3501UB
Safe operating area (clamped switching)	T_A = +25°C	
	I_B = 85 mA dc; I_C = 500 mA dc	2N3498, 2N3499
	I_B = 50 mA dc; I_C = 300 mA dc	2N3500, 2N3501, 2N3501UB

Outline Drawing (TO-5, TO-39)



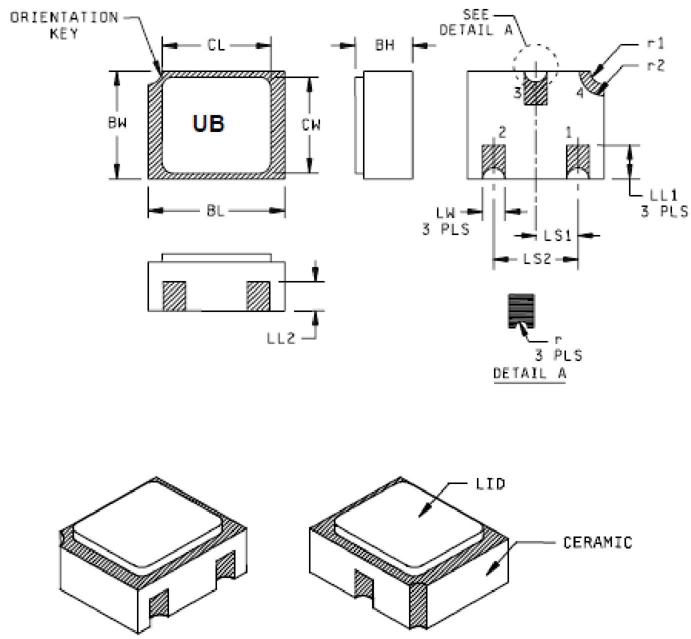
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7
LL	See notes 7, 12, and 13				
LU	.016	.019	0.41	0.48	7, 13
L_1		.050		1.27	13
L_2	.250		6.35		13
TL	.029	.045	0.74	1.14	3
TW	.028	.034	0.71	0.86	10, 11
P	.100		2.54		5
Q		.050		1.27	4
r		.010		.25	11
α	45° TP		45° TP		6

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LD applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Lead diameter shall not exceed .042 inch (1.07 mm) within L_1 and beyond LL minimum.
8. Lead designation, shall be as follows: 1 - emitter, 2 - base, 3 - collector.
9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. Symbol r applied to both inside corners of tab.
12. For transistor types 2N3498, 2N3499, 2N3500, and 2N3501, LL = .50 inch (12.7 mm) minimum and .750 inch (19.1 mm) maximum. For transistor types 2N3498L, 2N3499L, 2N3500L, and 2N3501L, LL = 1.50 inches (38.1 mm) minimum and 1.750 inches (44.5 mm) maximum.
13. All three leads.
14. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions (similar to TO-5, TO-39).

Outline Drawing (UB)



Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.97	
LL2	.017	.035	0.43	0.89	

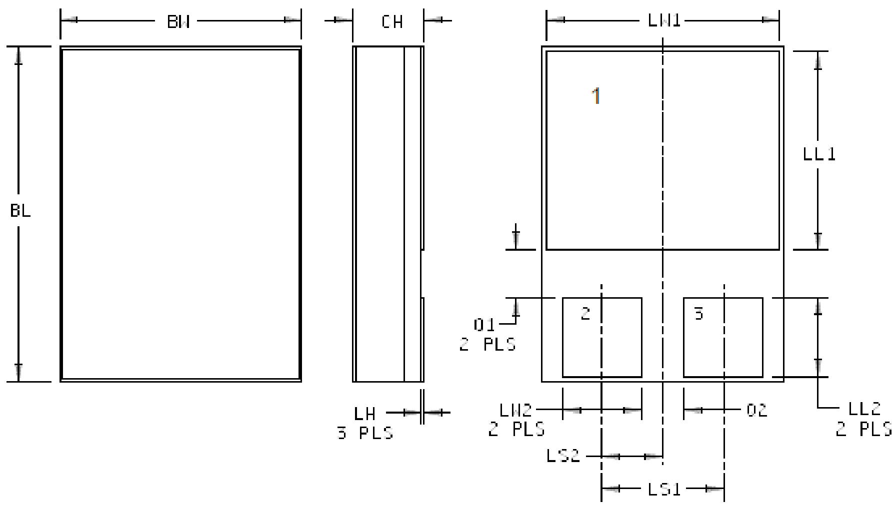
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LS_1	.036	.040	0.91	1.02	
LS_2	.071	.079	1.80	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas.
4. Lid material: Kovar.
5. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions, surface mount (2N3501UB version).

Outline Drawing (U4)

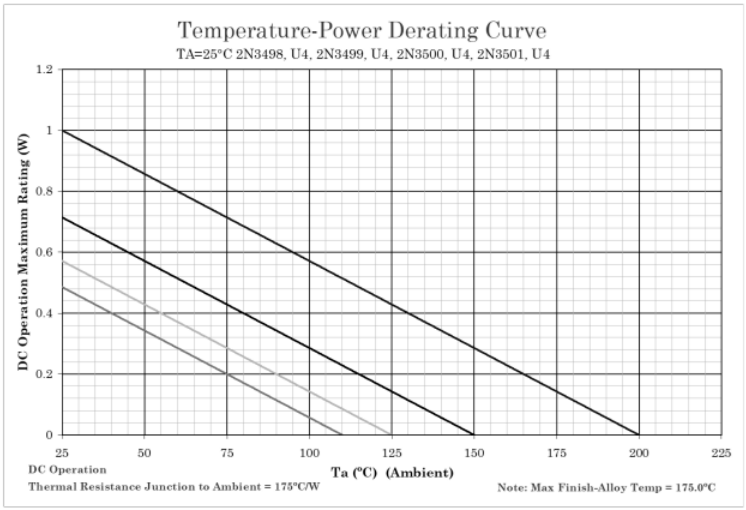


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.215	.225	5.46	5.72
BW	.145	.155	3.68	3.94
CH	.049	.075	1.24	1.91
LH		.020		0.51
LW1	.135	.145	3.43	3.68
LW2	.047	.057	1.19	1.45
LL1	.085	.125	2.16	3.18
LL2	.045	.075	1.14	1.91
LS1	.070	.095	1.78	2.41
LS2	.035	.048	0.89	1.22
Q1	.030	.070	0.76	1.78
Q2	.020	.035	0.51	0.89
1	Collector			
2	Base			
3	Emitter			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Terminal 1 is collector.
4. Terminal 2 is base.
5. Terminal 3 is emitter.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

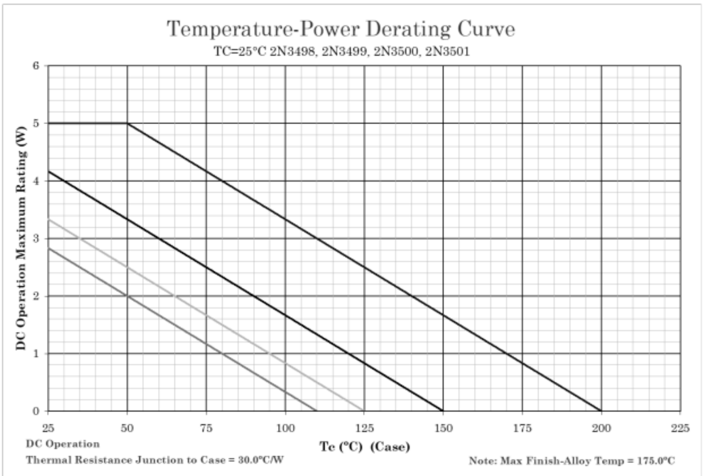
FIGURE 3. Physical dimensions and configuration U4.

Temperature-Power Derating Curves



NOTES:
1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

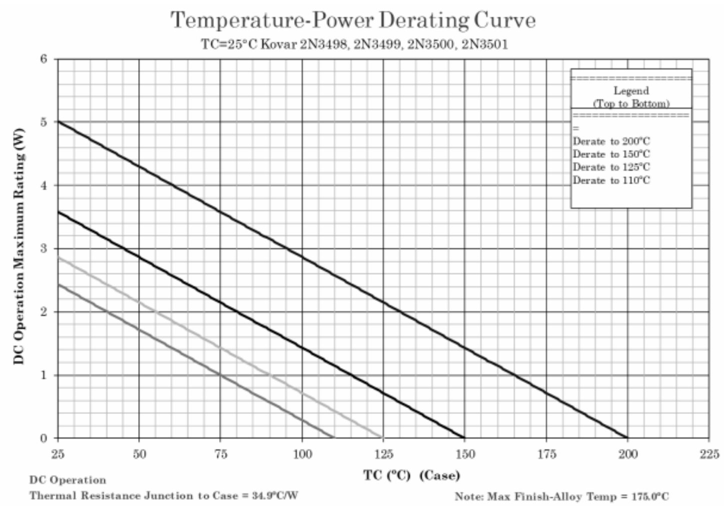
FIGURE 7. Derating for all devices ($R_{\theta JA}$) for 2N3498, 2N3499, 2N3500, and 2N3501 type devices.



NOTES:
1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8a. Derating for all devices ($R_{\theta JC}$) for 2N3498, 2N3499, 2N3500, and 2N3501 type devices.

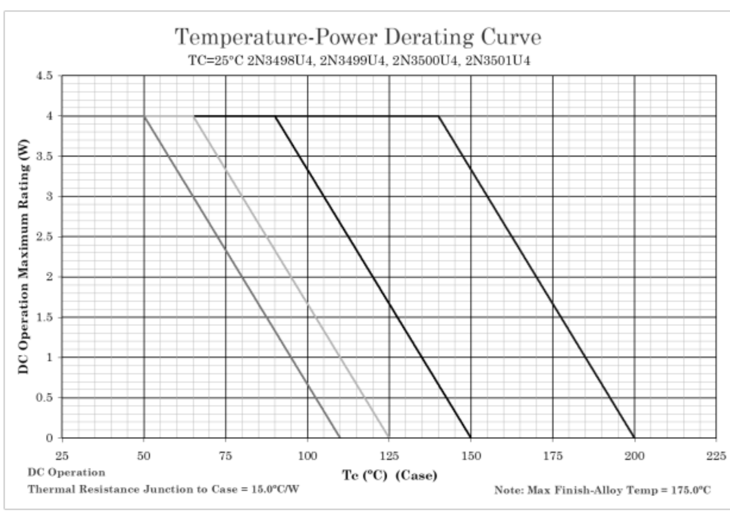
Temperature-Power Derating Curves



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8b. Derating for all devices ($R_{\theta JC,\ Kovar}$) for 2N3498, 2N3499, 2N3500, and 2N3501 type devices.

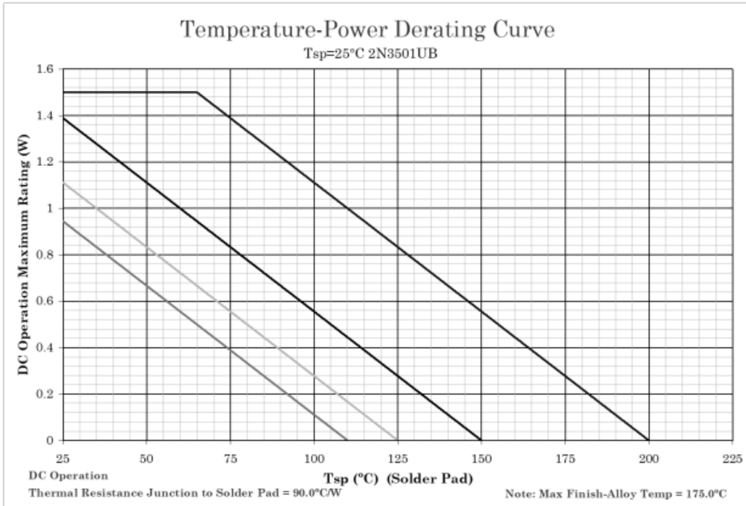


NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 9. Derating for all device ($R_{\theta JC}$) for 2N3498U4, 2N3499U4, 2N3500U4, and 2N3501U4 surface mount device.

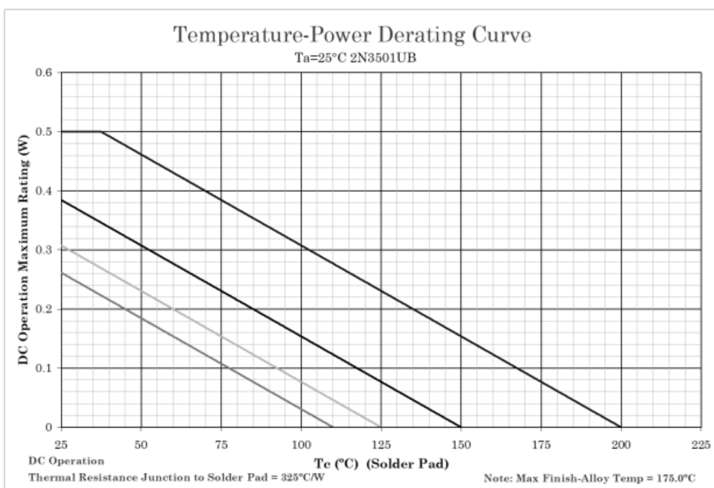
Temperature-Power Derating Curves



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 10. Derating for all devices ($R_{\theta JSP}$) for 2N3501UB type devices.

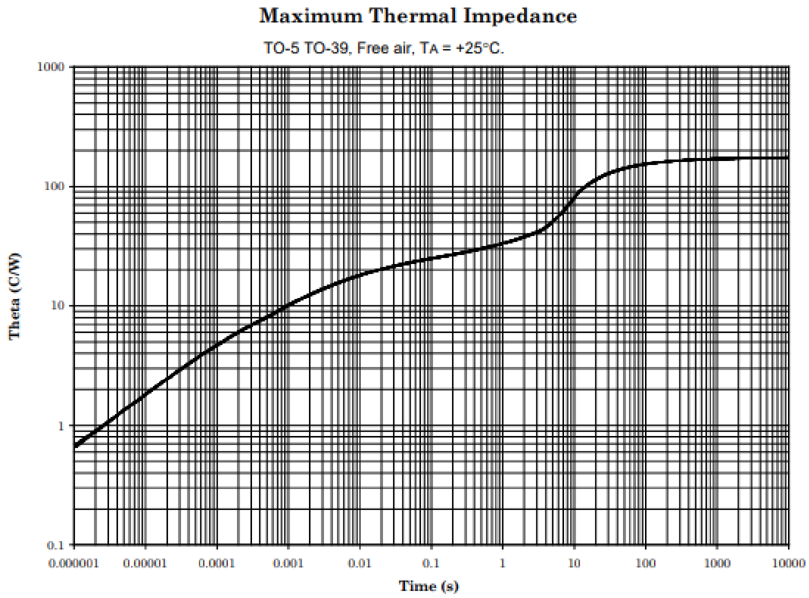


NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

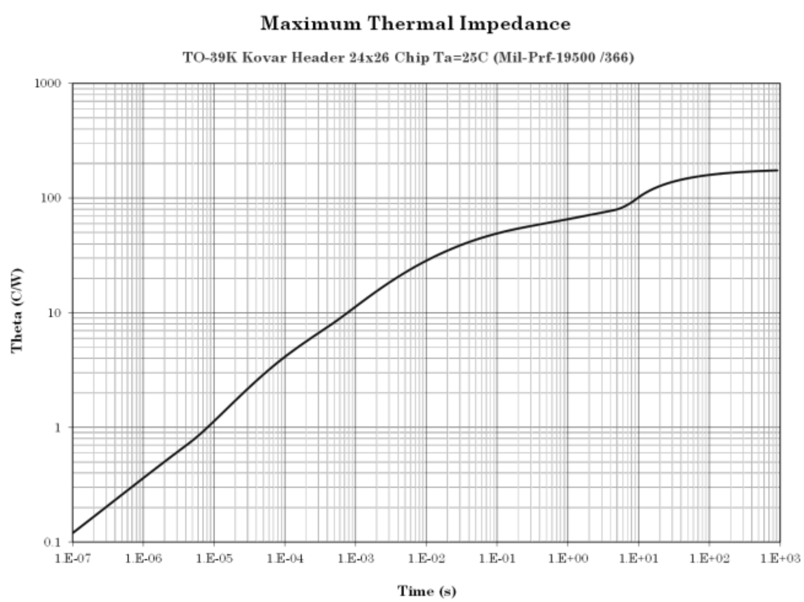
FIGURE 11. Derating for all devices ($R_{\theta JA}$) for 2N3501UB type devices.

Thermal Impedance Curves



Resistance $R_{\theta JA}$ = 175°C/W.

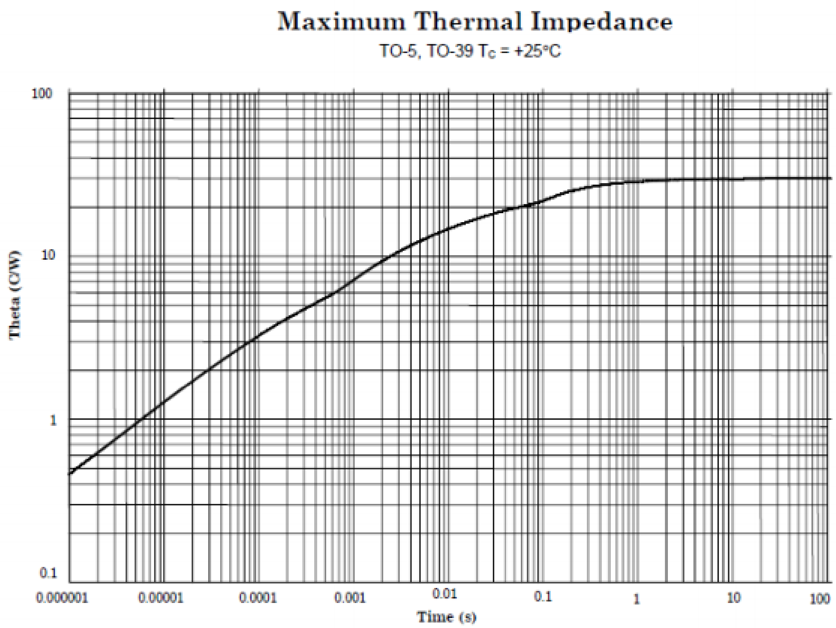
FIGURE 12. Thermal impedance graph ($R_{\theta JA}$) for 2N3498, 2N3499, and 2N3500.



Resistance $R_{\theta JA}$ = 175°C/W.

FIGURE 12 a. Thermal impedance graph ($R_{\theta JA}$) for Kovar 2N3498, 2N3499, and 2N3500.

Thermal Impedance Curves



Thermal resistance $R_{\theta JC}$ = 30°C/W

FIGURE 13. Thermal impedance graph $R_{\theta JC}$ for 2N3498, 2N3499, 2N3500, 2N3501, and all L devices.

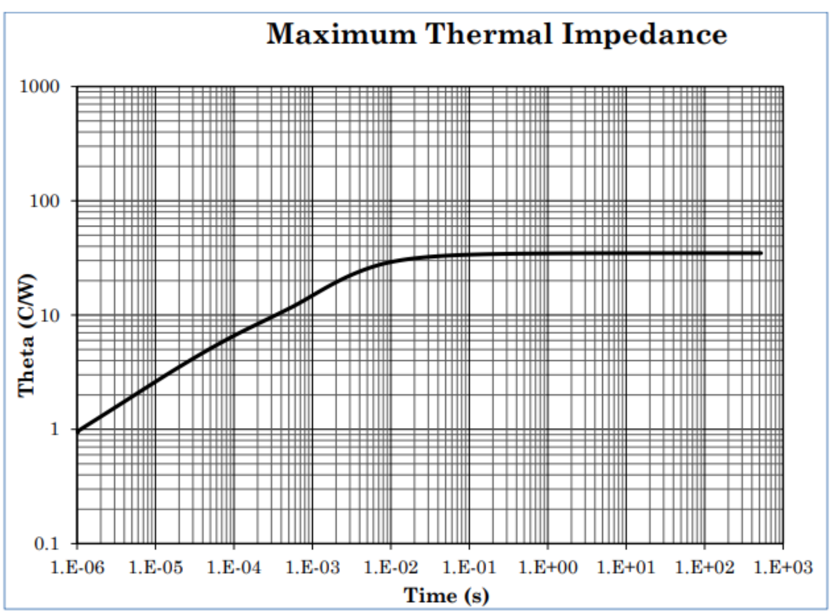
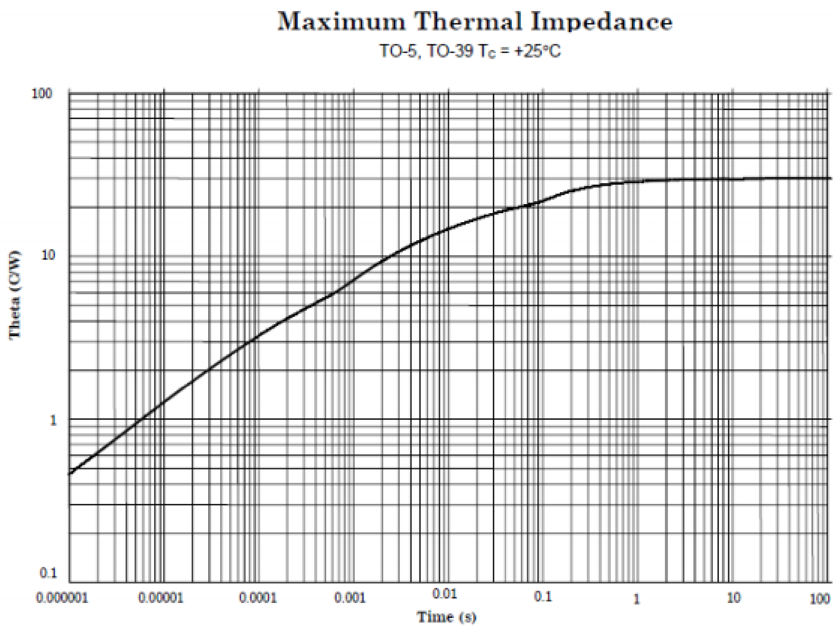


FIGURE 13a. Thermal impedance graph $R_{\theta JC}$ for Kovar 2N3498, 2N3499, 2N3500, 2N3501, and all L devices.

Thermal Impedance Curves



Thermal resistance $R_{\theta JC}$ = 30°C/W

FIGURE 13. Thermal impedance graph $R_{\theta JC}$ for 2N3498, 2N3499, 2N3500, 2N3501, and all L devices.

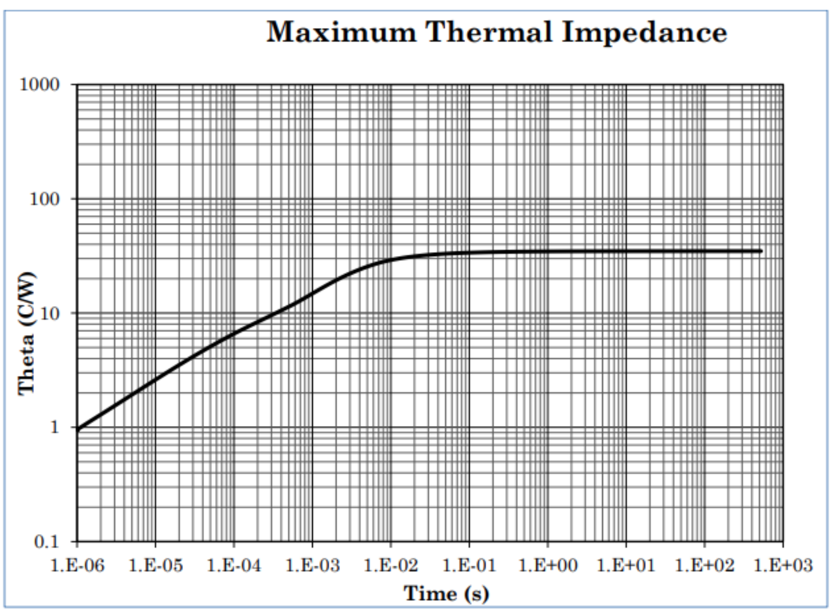
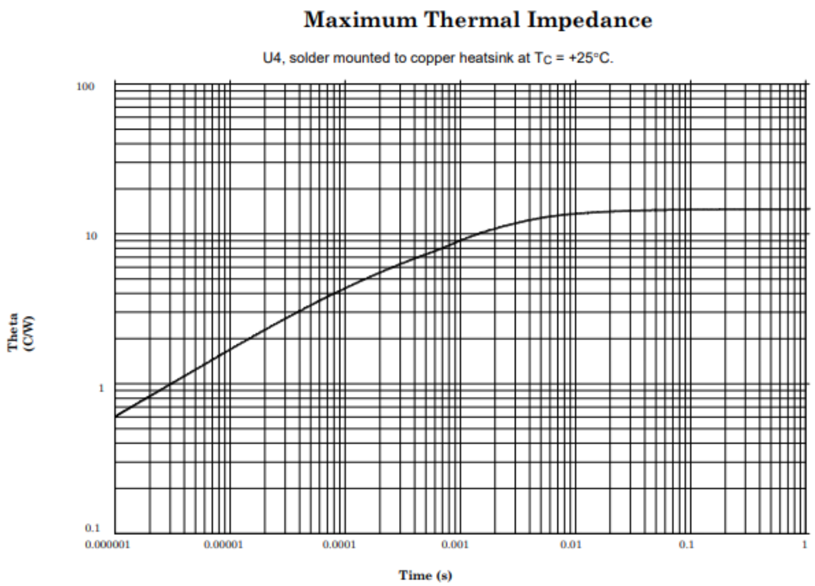


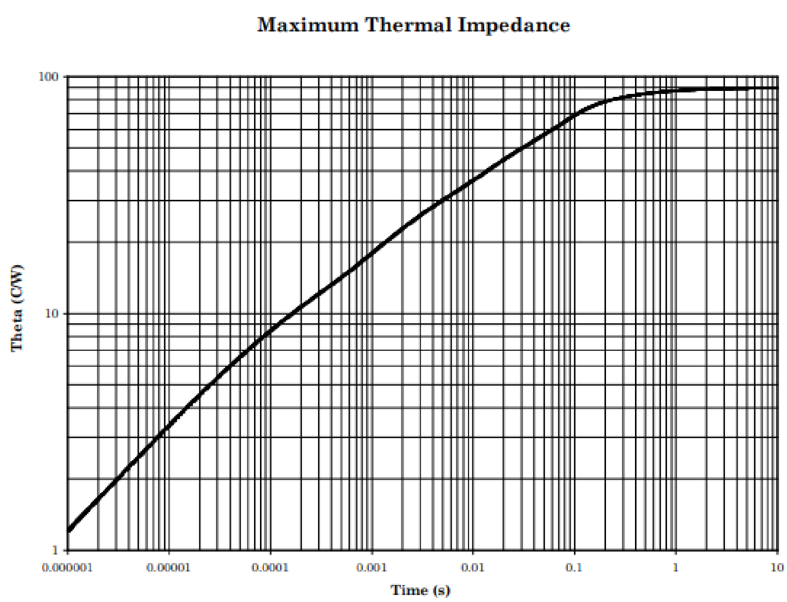
FIGURE 13a. Thermal impedance graph $R_{\theta JC}$ for Kovar 2N3498, 2N3499, 2N3500, 2N3501, and all L devices.

Thermal Impedance Curves



Thermal resistance $R_{\theta JC}$ = 15°C/W

FIGURE 14. Thermal impedance graph ($R_{\theta JC}$) for 2N3498U4, 2N3499U4, 2N3500U4, and 2N3501U4 (U4).



Thermal resistance $R_{\theta JSP}$ = 90°C/W

FIGURE 15. Thermal impedance graph ($R_{\theta JSP}$) for 2N3501UB (UB).

Thermal Impedance Curves

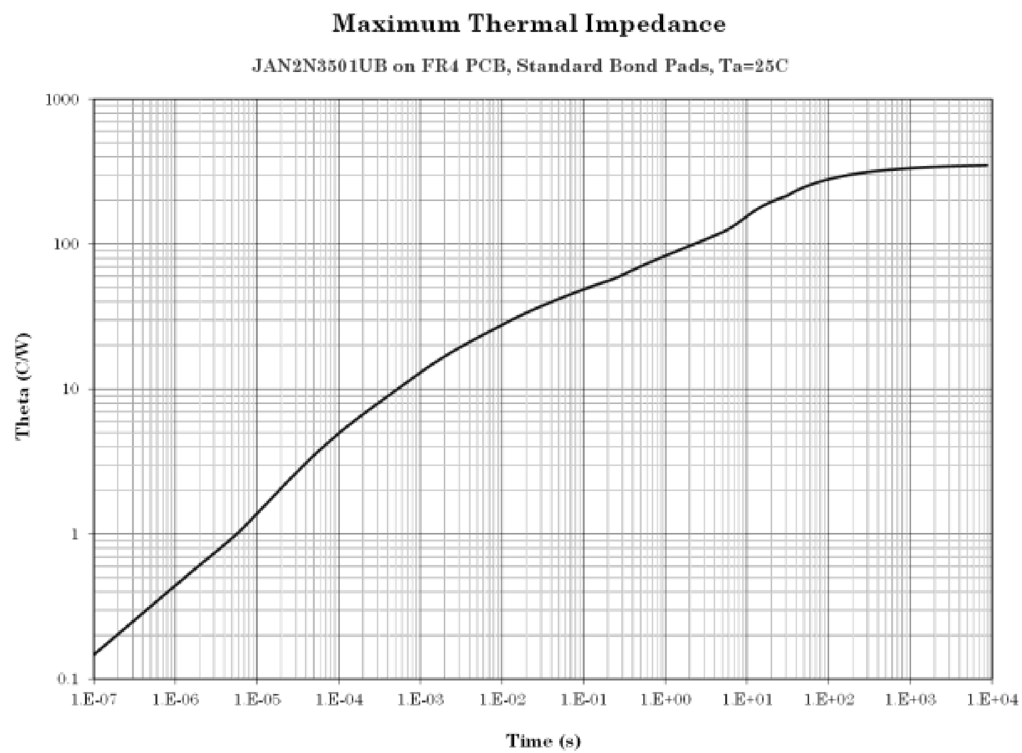


FIGURE 16. Thermal impedance graph ($R_{\theta JAPCB}$) for 2N3501UB (UB).