2N2906A, L, UA, UB
2N2907A, L, UA, UB

Radiation Hardened PNP Silicon Switching Transistors

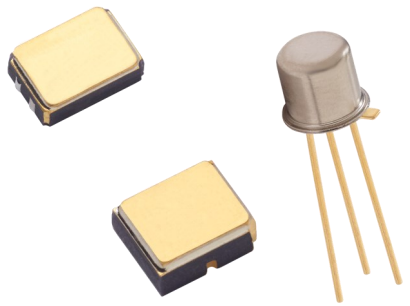
Rev. V3

Features

- Qualified to MIL-PRF-19500/291
- Available in JAN, JANTX, JANTXV, JANS and JANSR
- Rad Hard Levels M, D, P, L and R
- TO-18, Surface Mount UA & UB Packages

Applications

- Switching and Linear Applications
- DC and VHF Amplifier Applications



Electrical Specifications (T_A = 25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Minimum	Maximum
Collector - Emitter Breakdown	I_C = -10 mA dc	$V_{(BR)CEO}$	V dc	-60	—
Collector - Base Cutoff Current	V_{CB} = -60 V dc V_{CB} = -50 V dc	I_{CBO1} I_{CBO2}	µA dc nA dc	—	-10 -10
Emitter - Base Cutoff Current	V_{EB} = -5.0 V dc V_{EB} = -4.0 V dc	I_{EBO1} I_{EBO2}	µA dc nA dc	—	-10 -50
Collector - Emitter Cutoff Current	V_{CE} = -50 V dc	I_{CES}	nA dc	—	-50
Forward Current Transfer Ratio	2N2906A, L, UA, UB V_{CE} = -10 V dc: I_C = -0.1 mA dc V_{CE} = -10 V dc; I_C = -1.0 mA dc V_{CE} = -10 V dc; I_C = -10.0 mA dc V_{CE} = -10 V dc; I_C = -150.0 mA dc V_{CE} = -10 V dc; I_C = -500.0 mA dc 2N2907A, L, UA, UB V_{CE} = -10 V dc; I_C = -0.1 mA dc V_{CE} = -10 V dc; I_C = -1.0 mA dc V_{CE} = -10 V dc; I_C = -10.0 mA dc V_{CE} = -10 V dc; I_C = -150.0 mA dc V_{CE} = -10 V dc; I_C = -500.0 mA dc	h_{FE}		 40 40 40 40 40 75 100 100 100 50	 — 175 — 120 — — 450 — 300 —
Collector - Base Cutoff Current	I_C = -150 mA dc, I_B = -15 mA dc I_C = -500 mA dc, I_B = -50 mA dc	$V_{CE(sat)1}$ $V_{CE(sat)2}$	V dc	—	-0.4 -1.6
Base - Emitter Saturation Voltage	I_C = -150 mA dc, I_B = -15 mA dc I_C = -500 mA dc, I_B = -50 mA dc	$V_{BE(sat)1}$ $V_{BE(sat)2}$	V dc	-0.6 —	-1.3 -2.6
Collector - Base Cutoff Current	T_A = +150°C V_{CB} = -50 V dc	I_{CBO3}	µA dc	—	-10
Forward Current Transfer Ratio	T_A = -55°C V_{CE} = -10 V dc: I_C = -10 mA dc 2N2906A 2N2907A	h_{FE6}	-	 20 50	

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Radiation Hardened PNP Silicon Switching Transistors

Electrical Specifications (T_A = 25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Minimum	Maximum
Dynamic Characteristics:					
Small-Signal Short-Circuit Forward Current Transfer Ratio	V_{CE} = -10 V dc; I_C = -1.0 mA dc; f = 1 kHz 2N2906A, L, UA, UB 2N2907A, L, UA, UB	h_{fe}		40 100	—
Magnitude of Small-Signal Short-Circuit, Forward Current Transfer Ratio	V_{CE} = -20 V dc; I_C = -20 mA dc; f = 100 MHz	$\lvert h_{fe} \rvert$		2.0	—
Open Circuit Output Capacitance	V_{CB} = -10 V dc; I_E = 0, 100 kHz ≤ f ≤ 1 MHz	C_{obo}	pF	—	8
Input Capacitance (Output Open-Circuited)	V_{EB} = -2.0 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}	pF	—	30
Switching Characteristics:					
Saturated Turn-On Time	(See figure 16 of MIL-PRF-19500/291)	t_{on}	ns	—	45
Saturated Turn-Off Time	(See Figure 17 of MIL-PRF-19500/291)	t_{off}	ns	—	300

Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage	V_{CEO}	-60 V dc
Collector - Base Voltage	V_{CBO}	-60 V dc
Emitter - Base Voltage	V_{EBO}	-5 V dc
Collector Current	I_C	-600 mA dc
Operating & Storage Temperature Range	T_J, T_{STG}	-65°C to +200°C

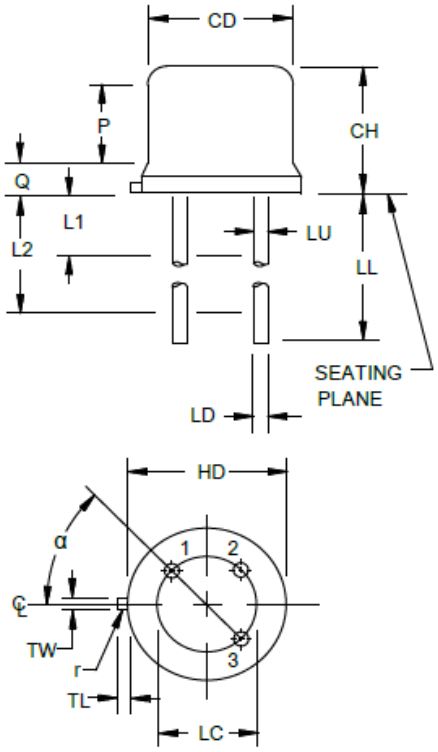
Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Types	P_T T_A = +25°C (1) (2)	P_T T_C = +25°C (1) (2)	P_T $T_{SP(IS)}$ = +25°C (1) (2)	P_T $T_{SP(AM)}$ = +25°C (1) (2)	$R_{\theta JA}$ (2) (3)	$R_{\theta JC}$ (2) (3)	$R_{\theta JSP(IS)}$ (2) (3)	$R_{\theta JSP(AM)}$ (2) (3)
	W	W	W	W	°C/W	°C/W	°C/W	°C/W
2N2906A, L,	0.5	1.0	N/A	N/A	325	150	N/A	N/A
2N2907A, L	0.5	1.0	N/A	N/A	325	150	N/A	N/A
2N2906AUA,	(4) 0.5	N/A	1.0	1.5	(4) 325	N/A	110	40
2N2907AUA	(4) 0.5	N/A	1.0	1.5	(4) 325	N/A	110	40
2N2906AUB, and UBN	(4) 0.5	N/A	1.0	N/A	(4) 325	N/A	90	N/A
2N2907AUB and UBN	(4) 0.5	N/A	1.0	N/A	(4) 325	N/A	90	N/A
2N2906AUBC and UBCN	(4) 0.5	N/A	1.0	N/A	(4) 325	N/A	90	N/A
2N2907AUBC and UBCN	(4) 0.5	N/A	1.0	N/A	(4) 325	N/A	90	N/A

(1) For derating, see figures 7, 8, 9, 10 and 11 of MIL-PRF-19500/291
(2) For abbreviations please see paragraph 3.3 of MIL-PRF-19500/291
(3) For thermal curves, see figures 12, 13, 14, 15 and 16 of MIL-PRF-19500/291
(4) For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute figures 7 and 12 for the UA, UB, UBC and UBCN package and use $R_{\theta JA}$

Outline Drawing (TO-18):

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	4
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	4
LC	.100 TP		2.54 TP		5
LD	.016	.021	0.41	0.53	6, 7
LL	.500	.750	12.70	19.05	6, 7, 8
LU	.016	.019	0.41	0.48	6, 7
L1		.050		1.27	6, 7
L2	.250		6.35		6, 7
P	.100		2.54		
Q		.030		0.76	4
TL	.028	.048	0.71	1.22	9
TW	.036	.046	0.91	1.17	10
r		.010		0.25	11
α	45° TP		45° TP		5

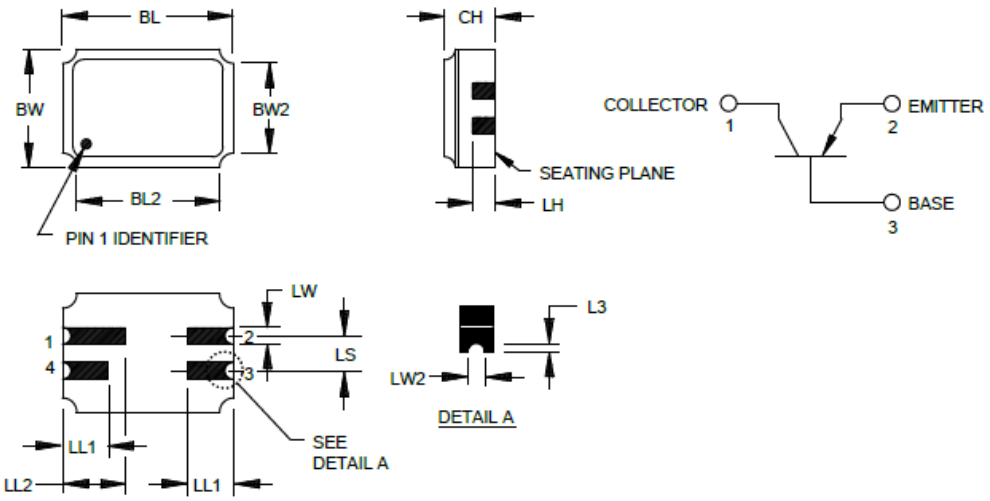


NOTES:

1. Dimension are in inches. Millimeters are given for general information only.
2. Terminal 1 = emitter, terminal 2 = base, terminal 3 = collector.
3. The collector shall be internally connected to the case.
4. Body contour optional within zone defined by dimensions CD, HD, and Q.
5. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
6. Dimension LU applies between dimensions L1 and L2. Dimension LD applies between dimensions L2 and LL minimum. Diameter is uncontrolled in dimension L1 and beyond dimension LL minimum.
7. All three leads.
8. For "L" suffix devices, dimension LL = 1.5 inches (38.10 mm) minimum and 1.75 inches (44.45 mm) maximum.
9. Dimension TL measured from maximum HD.
10. Beyond r (radius) maximum, dimension TW shall be held for a minimum length of .011 inch (0.28 mm).
11. Dimension r (radius) applies to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for TO-206AA package (similar to TO-18).

Outline Drawing (UA Surface Mount):



Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.90	3
L3	.003		0.08		5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Terminal 1 = collector, terminal 2 = emitter, terminal 3 = base, terminal 4 = not connected.
3. Dimension "CH" controls the overall package thickness. When a window lid is used, dimension "CH" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions "LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW2" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15 mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions for 4 terminal SMD package (UA).

Outline Drawing (UB Surface Mount)

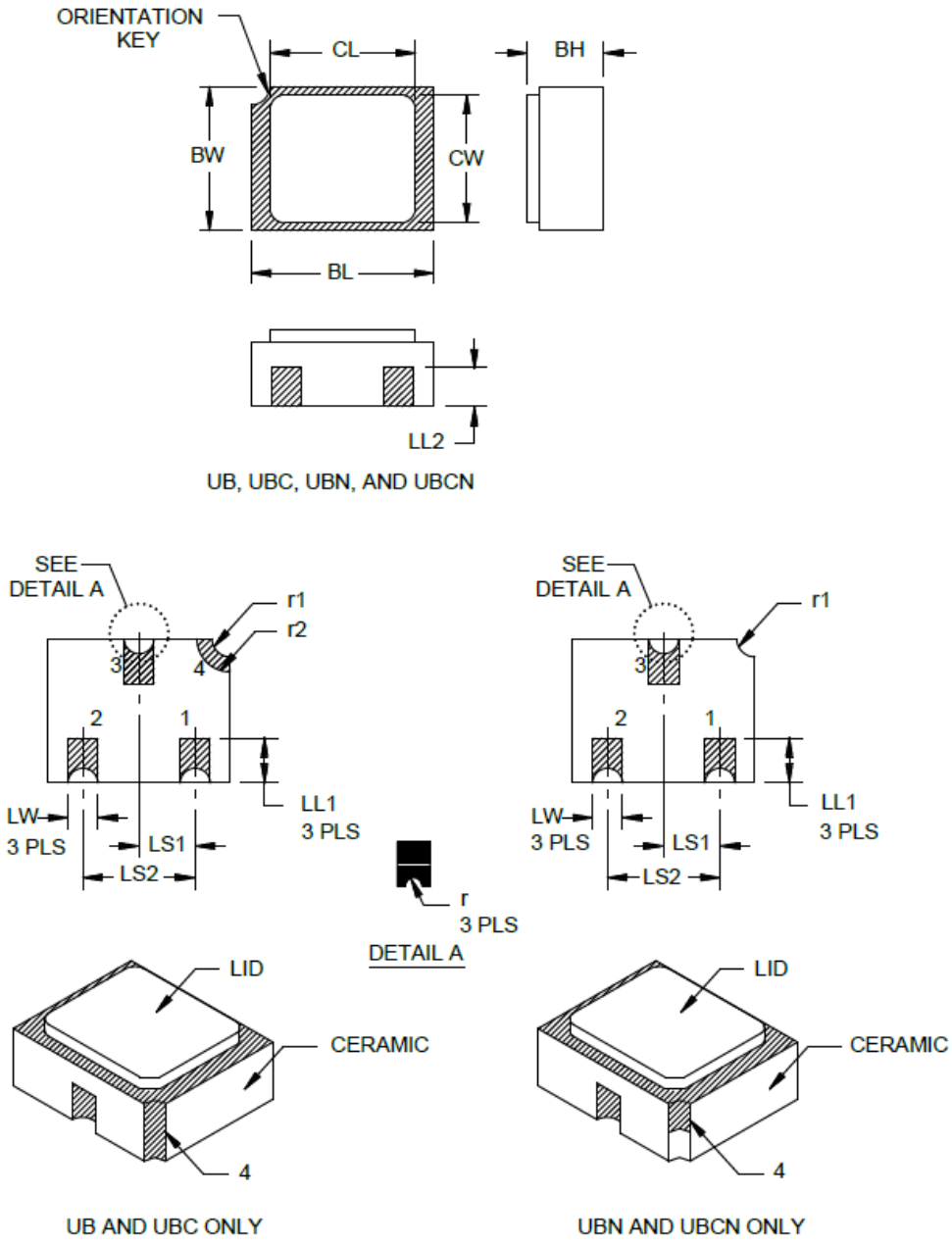


FIGURE 3. Physical dimensions for 3 and 4 terminal SMD packages (UB, UBN, UBC, and UBCN).

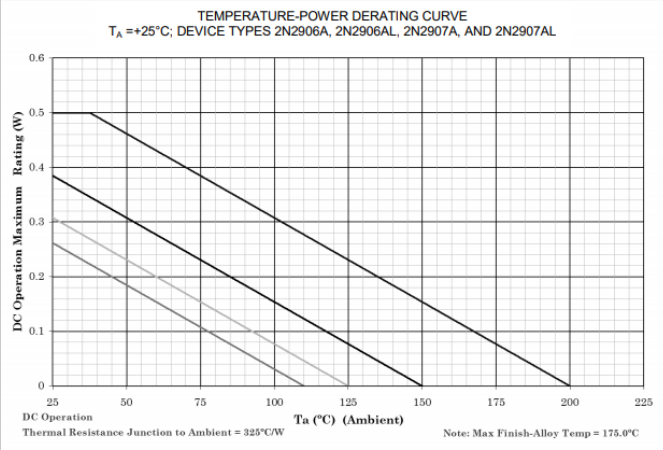
Outline Drawing (UB Surface Mount)

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
BH	.046	.056	1.17	1.42	UB only, 3
BH	.046	.056	1.17	1.42	UBN only, 4
BH	.055	.069	1.40	1.75	UBC only, 5
BH	.055	.069	1.40	1.75	UBCN only, 6
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.97	3 PLS
LL2	.014	.035	0.356	0.89	3 PLS
LS_1	.035	.040	0.89	1.02	
LS_2	.071	.079	1.80	2.01	
LW	.016	.024	0.41	0.61	
r		.008		0.20	5
r1		.012		0.30	7
r2		.022		0.56	UB and UBC only, 7

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Hatched areas on package denote metallized areas.
3. UB only: Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the metal lid.
4. UBN only: Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Isolated lid with three pads only.
5. UBC (ceramic lid) only: Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
6. UBCN (ceramic lid) only: Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Isolated lid with 3 pads only.
7. For design reference only.
8. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

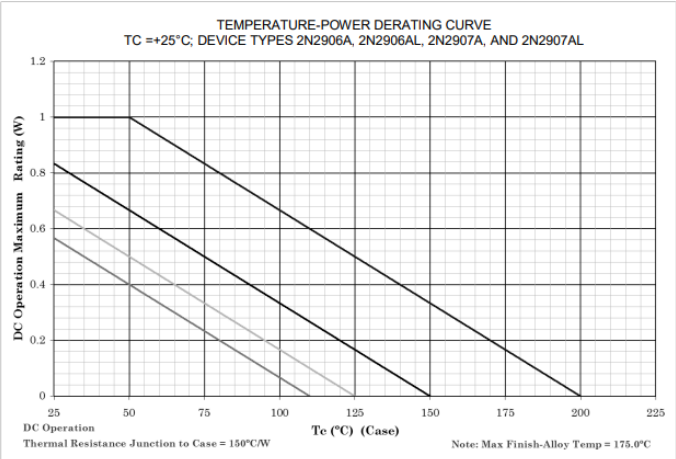
FIGURE 3. Physical dimensions for 3 and 4 terminal SMD packages (UB, UBN, UBC, and UBCN) – Continued.

Temperature-Power Derating Curves



NOTES:
1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

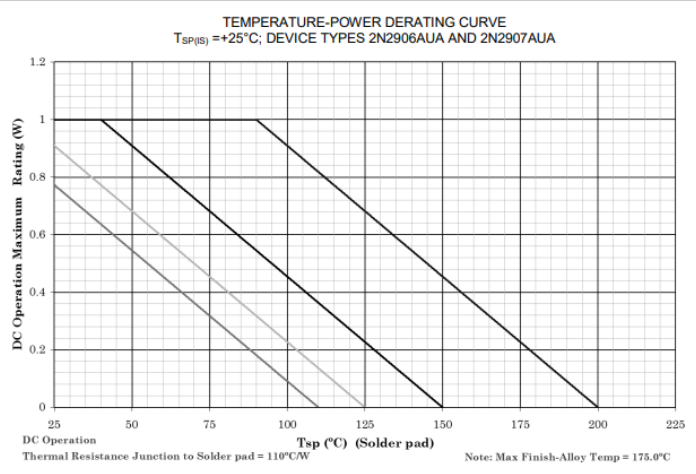
FIGURE 7. Temperature-power derating for TO-206AA package ($R_{\theta JA}$) leads .125 inch (3.18 mm) PCB.



NOTES:
1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

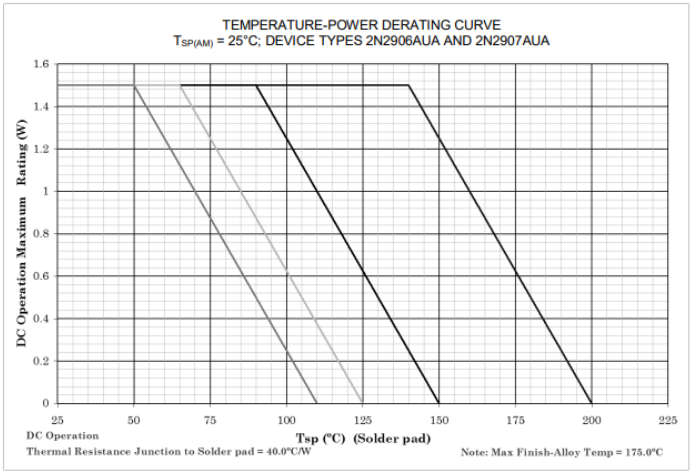
FIGURE 8. Temperature-power derating for TO-206AA package ($R_{\theta JC}$), base case mount.

Temperature-Power Derating Curves



NOTES:
1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

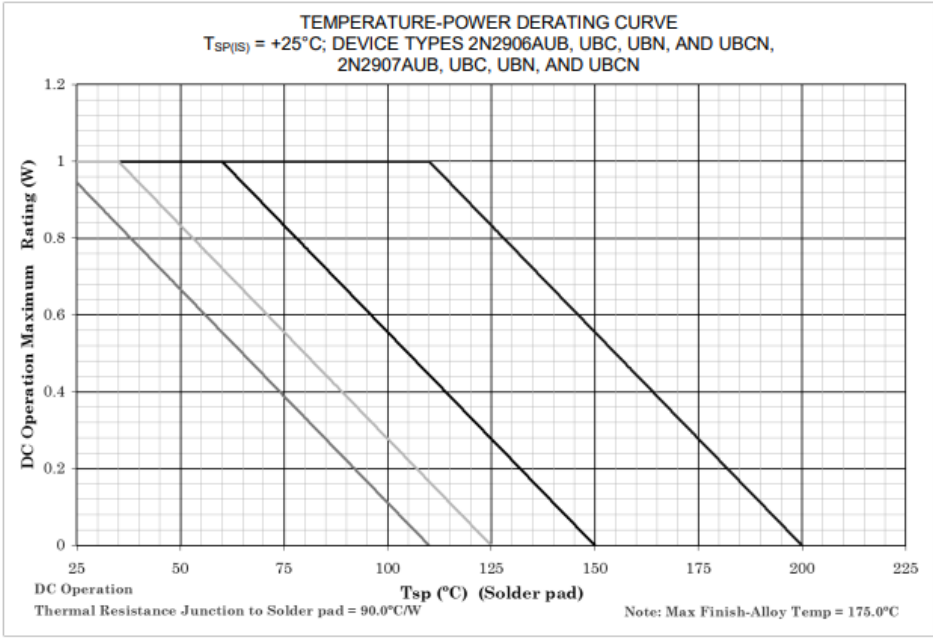
FIGURE 9. Temperature-power derating for UA package ($R_{\theta JSP(IS)}$), infinite sink 4-points.



NOTES:
1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 10. Temperature-power derating for UA package ($R_{\theta JSP(AM)}$) 4-point solder pad (adhesive mount to PCB).

Temperature-Power Derating Curves



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 11. Temperature-power derating for UB, UBC, UBN, or UBCN packages ($R_{\theta JSP(IS)}$) infinite sink 3-point.

Thermal Impedance Curves

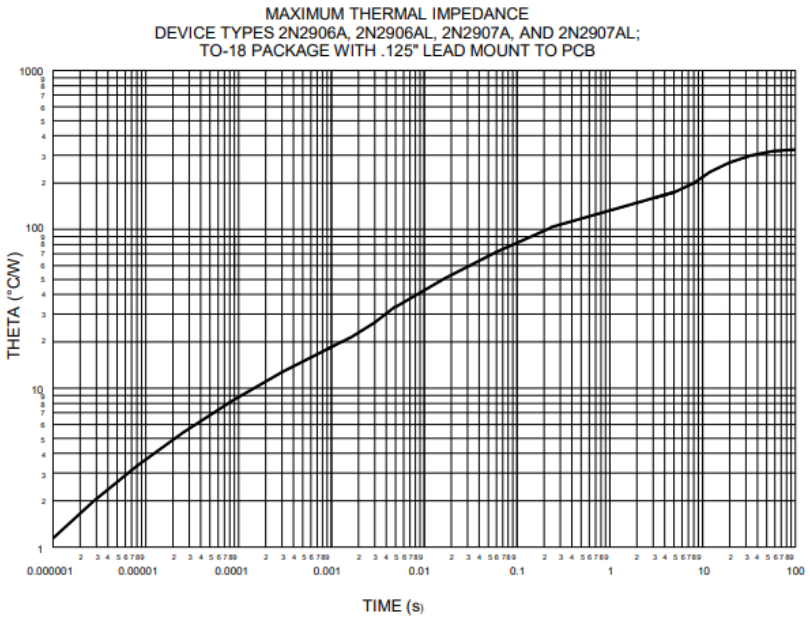


FIGURE 12. Thermal impedance graph ($R_{\theta JA}$) for devices in a TO-206AA package.

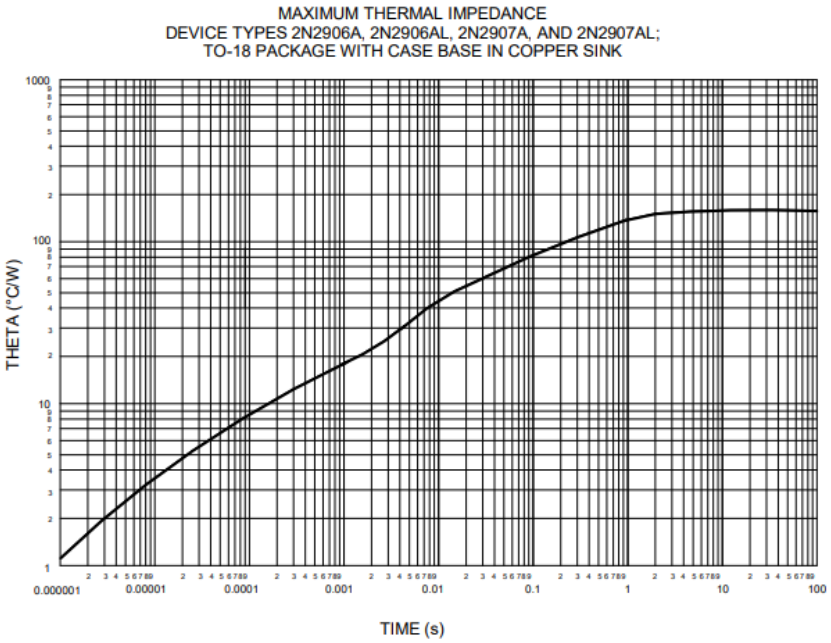


FIGURE 13. Thermal impedance graph ($R_{\theta JC}$) for devices in TO-206AA package.

Thermal Impedance Curves

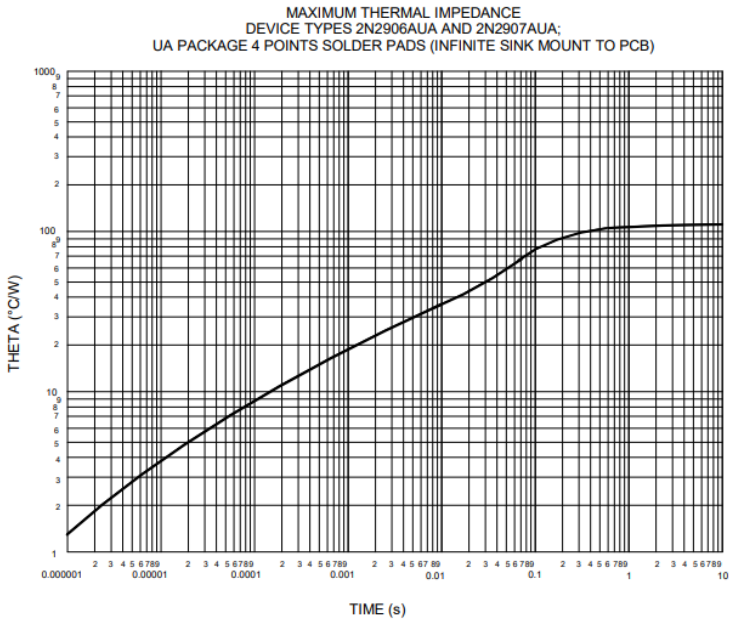


FIGURE 14. Thermal impedance graph ($R_{\theta JSP(IS)}$) for devices in a UA package.

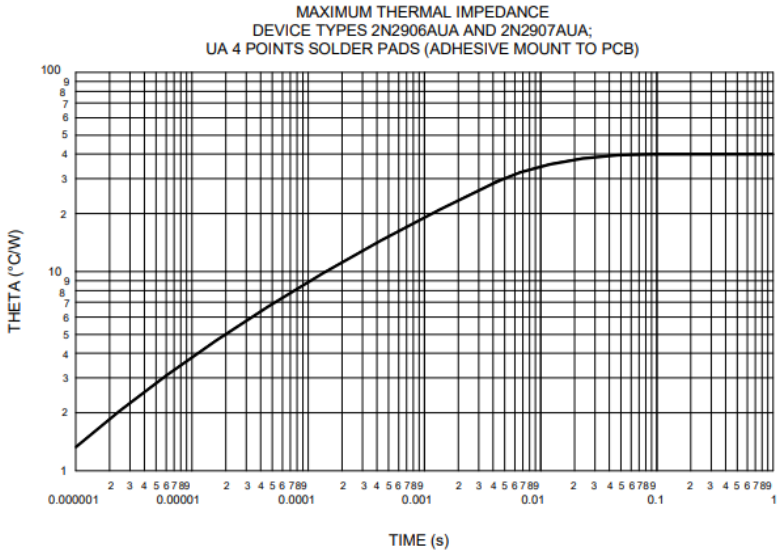


FIGURE 15. Thermal impedance graph ($R_{\theta JSP(AM)}$) for devices in a UA package.

Thermal Impedance Curves

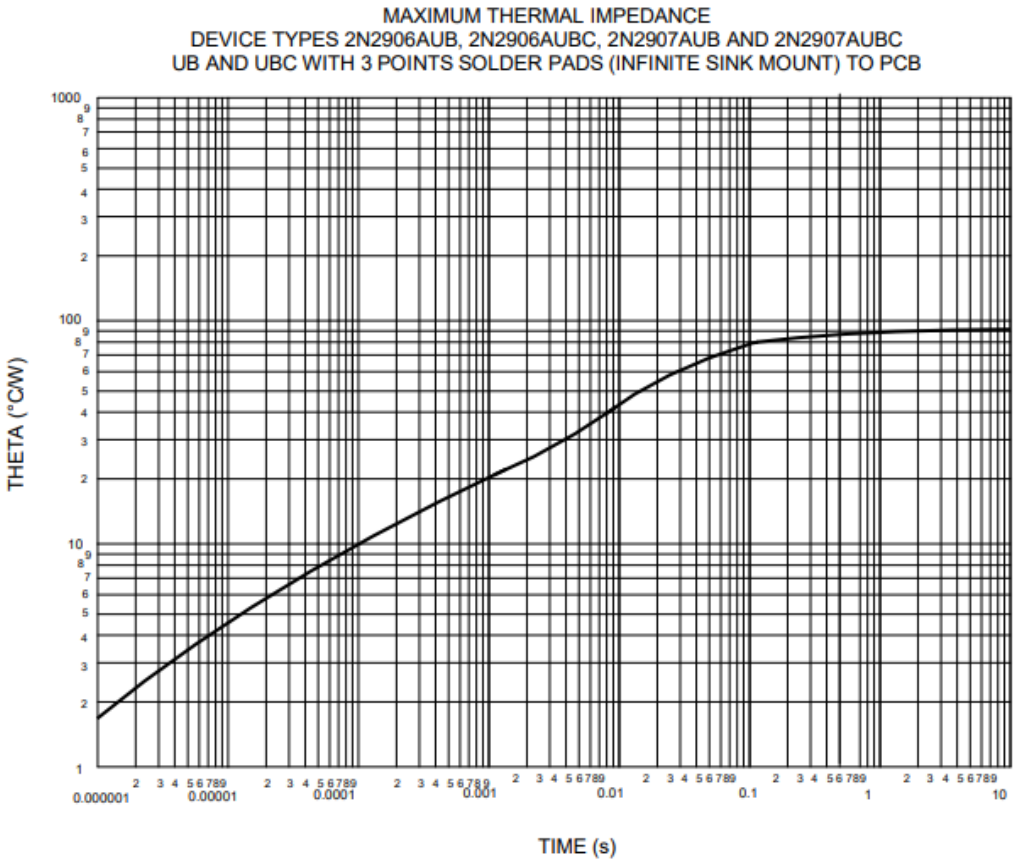


FIGURE 16. Thermal impedance graph ($R_{\theta JSP(JS)}$) for devices in a UB, UBC, UBN, and UBCN package).