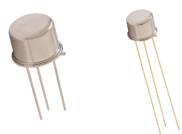
## **NPN Low Power Silicon Transistor**



Rev. V2

#### Features

- JAN, JANTX, JANTXV, JANS and JANSR Qualified to MIL-PRF-19500/391
- Lightweight & Low Power
- Ideal for Space, Military, & Other High Reliability Applications
- Available in TO-5 and TO-39 packages



## Electrical Characteristics (T<sub>A</sub> = +25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Breakdown Voltage	I <sub>C</sub> = 30 mA	V <sub>(BR)CEO</sub>	V dc	80	_
Collector - Base Cutoff Current	V <sub>CB</sub> = 140 V	I <sub>CBO1</sub>	µA dc	—	10
Emitter - Base Cutoff Current	V <sub>EB</sub> = 7 V	I <sub>EBO1</sub>	µA dc	—	10
Collector - Emitter Cutoff Current	V <sub>CE</sub> = 90 V	I <sub>CES1</sub>	nA dc	—	10
Emitter - Base Cutoff Current	V <sub>EB</sub> = 5 Vdc	I <sub>EBO2</sub>	nA dc	—	10
Forward Current Transfer Ratio		h <sub>FE1</sub> h <sub>FE2</sub> h <sub>FE3</sub> h <sub>FE4</sub> h <sub>FE5</sub>	-	100 50 90 50 15	300 300 300
Collector - Emitter Saturation Voltage	$I_{C}$ = 150 mA; $I_{B}$ = 15 mA $I_{C}$ = 500 mA; $I_{B}$ = 50 mA	V <sub>CE(SAT)1</sub> V <sub>CE(SAT)2</sub>	V dc	_	0.2 0.5
Base - Emitter Saturation Voltage	I <sub>C</sub> = 150 mA; I <sub>B</sub> = 15 mA	$V_{\text{BE(SAT)}}$	V dc	_	1.1
Collector - Emitter Cutoff Current	T <sub>A</sub> = +150°C V <sub>CE</sub> = 90 V	I <sub>CES2</sub>	µA dc	_	5
Forward Current Transfer Ratio	$T_{A} = -55^{\circ}C$ $V_{CE} = 10 V dc; I_{C} = 150 mA dc$	h <sub>FE6</sub>		40	

Safe Operating Area	
DC Tests:	T <sub>C</sub> = +25°C; 1Cycle, t = 10 ms
Test 1:	$V_{CE}$ = 10 V, I <sub>C</sub> = 500 mA dc
Test 2:	$V_{CE}$ = 40 V, I <sub>C</sub> = 130 mA dc
Test 3:	$V_{CE}$ = 80 V, I <sub>C</sub> = 60 mA dc

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Parameter	Test Conditions	Symbol	Units	Min.	Max.		
Dynamic Characteristics							
Small-Signal Short-Circuit Forward -Current Transfer Ratio	$V_{CE}$ = 5 V dc; I <sub>C</sub> = 1 mA dc; f = 1 kHz	h <sub>FE</sub>		80	400		
Magnitude of Small-Signal Short-Circuit Forward Current Transfer Ratio	$V_{CE}$ = 10 V dc; I <sub>C</sub> = 50 mA dc; f = 20 MHz	h <sub>FE</sub>		5	20		
Input Capacitance (Output Open Circuited)	$V_{EB}$ = 0.5 V dc; $I_{C}$ = 0; 100 kHz $\leq$ f $\leq$ 1 MHz	C <sub>ibo</sub>	pF		60		
Open Circuit Output Capacitance	V <sub>CB</sub> = 10 V dc; I <sub>E</sub> = 0; 100 kHz ≤ f ≤ 1 MHz	C <sub>obo</sub>	pF	_	12		
Noise Figure	$V_{CE}$ = 10 V dc; I <sub>C</sub> = 100 µA dc; Rg = 1 kΩ; power bandwidth = 200 H <sub>Z</sub> f = 1 kHz	NF	dB	_	4		
Pulse Response	See Figure 21 of MIL-PRF-19500/391	t <sub>on</sub> +t <sub>off</sub>	ns		30		

## Absolute Maximum Ratings ( $T_A = +25^{\circ}C$ unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage	$V_{CEO}$	80 V dc
Collector - Base Voltage	V <sub>CBO</sub>	140 V dc
Emitter - Base Voltage	$V_{\text{EBO}}$	7 V dc
Collector Current	Ι <sub>C</sub>	1 A dc
Total Power Dissipation @ $T_A = 25^{\circ}C$ @ $T_C = 25^{\circ}C$	P <sub>T</sub> <sup>(1)(2)</sup>	0.8 W 5.0 W
Operating & Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65°C to +200°C

### **Thermal Characteristics**

Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Case <sup>(2) (3)</sup>	$R_{ extsf{ heta}JC}$	30°C/W
Thermal Resistance, Junction to Ambient <sup>(2) (3)</sup>	$R_{ extsf{ heta}JA}$	195°C/W

(1) For derating, see figures 8, 9, 10, 11, 12 and 13 of MIL-PRF-19500/391
(2) See paragraph 3.3 of MIL-PRF-19500/391

(3) For thermal curves, see figures 14, 15, 16, 17, 18, 19 and 20 of MIL-PRF-19500/391

<sup>2</sup> 

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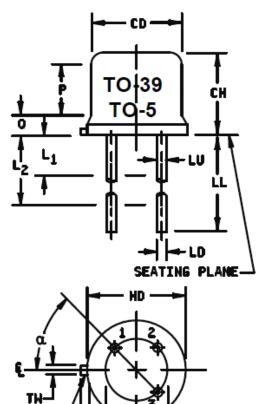
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### Outline Drawing (TO-5, TO-39)

Dimensions							
Symbol	Inc	Inches		Millimeters			
					Notes		
	Min	Max	Min	Max			
CD	.305	.335	7.75	8.51			
CH	.240	.260	6.10	6.60			
HD	.335	.370	8.51	9.40			
LC	.200	.200 TP 5.08 TP		.200 TP		3 TP	6
LD	.016	.021	0.41	0.53	7, 8		
LL	1.50	1.750	38.10	40.45	7, 8, 12		
LU	.016	.019	0.41	0.48	7, 8		
L <sub>1</sub>		.050		1.27	7, 8		
L <sub>2</sub>	.250		6.35		7, 8		
Q		.050		1.27	5		
TL	.029	.045	0.74	1.14	4		
TW	.028	.034	0.71	0.86	3		
r		.010		0.25	10		
α	45° TP		45° TP		6		
Р	.100		2.54				



#### NOTES:

- 1. Dimension are in inches.
- 2. Millimeters are given for general information only.
- 3. Beyond r (radius) maximum, TW shall be held for
- a minimum length of .011 (0.28 mm).
- Dimension TL measured from maximum HD.
   Body contour optional within zone defined by HD, CD, and Q.
- body control optional within 20th defined by 10, cb, and d.
   Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within
- .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
- Dimension LU applies between L1 and L2. Dimension LD applies between L2 and minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
- 8. All three leads.
- 9. The collector shall be internally connected to the case.
- 10. Dimension r (radius) applies to both inside corners of tab.
- 11. In accordance with ASME Y14.5M, diameters are equivalent to \$\phix\$ symbology.
- 12. For "S" suffix devices, dimension LL is 0.500 (12.70 mm) minimum, 0.750 (19.05 mm) maximum.
- 13. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
  - \* FIGURE 1. Physical dimensions for device types 2N3019 (TO-5) and 2N3019S (TO-39).

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### NPN Low Power Silicon Transistor



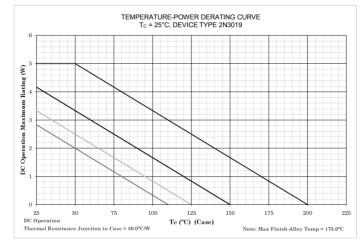
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#### TEMPERATURE-POWER DERATING CURVE T<sub>A</sub> = 25°C; DEVICE TYPE 2N3019 0. 0.8 € 0.7 Rating 0.6 imum 0.5 May 0.4 ration 0.3 Due 0.2 ä 0.1 0 75 25 50 100 125150 175 200 225DC Operation Ta (°C) (Ambient) Note: Max Finish-Alloy Temp = 175.0°C Thermal Resistance Junction to Ambient = 195°C/W

#### NOTES:

- This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_{J}$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T<sub>J</sub> allowed.
- 2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.) 3. Derate design curve chosen at  $T_J \leq +150^{\circ}$ C, where the maximum temperature of electrical test is
- performed. Derate design curve chosen at  $T_J \le +125^{\circ}$ C, and  $+110^{\circ}$ C to show power rating where most users want to limit  $T_J$  in their application. 4.

#### FIGURE 8. Derating for 2N3019 (R<sub>BJA</sub>) PCB (TO-5 and TO-39).



#### NOTES:

- This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq$  T<sub>J</sub> specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T<sub>J</sub> allowed.
- Derate design curve constrained by the maximum junction temperatures and power rating specified. (See
- 1.3 herein.) 3. Derate design curve chosen at  $T_J \le +150^{\circ}$ C, where the maximum temperature of electrical test is
- performed. Derate design curve chosen at  $T_J \le +125^{\circ}$ C, and +110°C to show power rating where most users want to limit  $T_J$  in their application. 4.
  - FIGURE 9. Derating for 2N3019 (Reuc), base case mounted (TO-5 and TO-39).

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### **Temperature-Power Derating Curve**

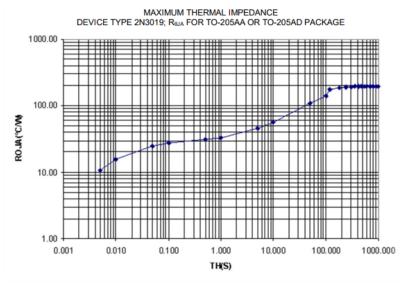
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### **NPN Low Power Silicon Transistor**



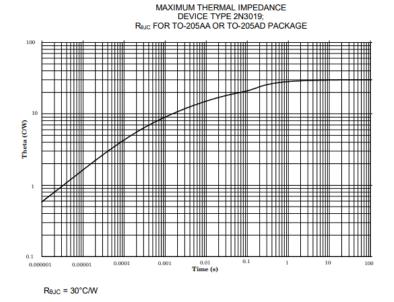
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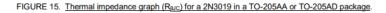
#### **Thermal Impedance Curve**



R<sub>0JA</sub> = 195°C/W

FIGURE 14. Thermal impedance graph (R<sub>BJA</sub>) for a 2N3019 in a TO-205AA or TO-205AD package.





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